marantz®

Model LC3701E / LC4201E

HDMI™ HIGH DEFINITION MULTIMEDIA INTERFACE

HDTV ready

1. FORWARD

This document defines the design and performance requirements for HYUNDAI IT E-SERIES MODEL 26" ,32",37",42",46" LCD COLOR TV

It is capable of displaying maximum 1366X768 resolution image.
The LCD TV screen comes equipped with a dedicated terminal board which is designed to a Accommodate an image signal from a variety of multimedia source such as DVD players,VCRs Camcoders and set-top box,CATV

2. GENERAL DESCRIPTION

2.1 Features

This digital Terrestrial receiver is suited for DVB-T standard reception of Free digital Terrestrial program and has the following features;

<iDTV Incase>

* Full DVB-T compliant
* High quality video and CD quality sound by MPEG-2 standard
* 3000 pre-programmable station (video:2000ch,audio;1000ch)
* User friendly and well –defined On Screen Display
* Parent lock and favorite select function
* EPG(Electronic Program Guide)Function
* Full infrared remote control
* Automatic scan for added channel
* NIT scan function
* Manual and automatic scan programming
* Display signal strength meter on the screen
* Optical connector for SPDIF Output
* Output for Audio L/R
* PIG (Picture in Graphic) function
* High resolution graphic with 256 colors
* Channel delete, move, edit and add function
* Software up grade with RS232C

<Others>

* There are 7 languages OSD as English, Deutsch, Français, Nederland, Italiano, Español, Suomi
  * A choice of WIDE, ZOOM and advanced 4:3 and 14:9 AUTO size aspect ratios
  * High luminance and contrast ratio, low reflection and wide viewing angle
  * PIP (Picture-In-Picture)
  * Auto Volume Limit
  * Noise Reduction
  * Sound Mode Setting(7 Equalizer : 100Hz,3200Hz,1.0KHz, 3.0KHz,10KHz)
  * Picture Mode Setting

* Full multimedia capability
* TELETEXT(252pages : only ATV)

2.3 General Specification

The LCD TV is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Flourscent Lamp(CCFL) backlight system.
The matrix employs a-Si Thin Film Transistor as the active element.
It is a transmissive display type which is operated in the normally black mode.
It has a 31.51 inch diagonally measured active display area with WXGA resolution.
(768 vertical by 1366 horizontal pixel array) Each pixel is divided into
Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes.
Gray scale or the luminance of the sub-pixel color is determined with
a 8-bit gray scale signal for each dot, Therefore it can present a palette
of more than 16.7M(true) Colors.
It has been designed to apply the 8Bit 1 port LVDS interface.
It is intended to support LCD TV, PCTV where high brightness,
super wide viewing angle, high color gamut, high color depth and fast response time are important

2.4 General Features(REFER 32")

Parameter	Specification			Unit	Remarks
Effective Display Size	697.6845(H) X 392.256(V)			mm	
Input Voltage	AC 100 ~ 240, 50/60Hz			V	
Display Type	Flat(LCD)				
Input Type	VIDEO INPUT			1	Audio L/R 1
	S-VIDEO INPUT			1	Audio Common with VIDEO 1
	COMPONENT INPUT			1	Audio L/R 2
	PC-VGA			1	Audio Common with DVI
	HDMI INPUT			1	DVI iinput compatible
	RS232			1	SERVICE
	SCART Input	Full	RGB,CVBS	1	Audio L/R1
		Half	CVBS	1	
Output Type	SCART Output	Full	Analog TV	1	Audio L/R1
		Half	CVBS	1	
	Composite CVBS			1	
	Audio out LR			1	
	Loud Speaker L/R			1	Audio L/R1
	SPDIF(Optical)			1	Audio
	SPDIF(Electrical)			1	Audio
Parameter	Specification			Unit	Remarks
Number of Pixels	1366X 768			pixels	
Pixel pitch	0.51075(H) X 0.51075(W)			mm	
Pixel arrangement	RGB Vertical stripe(Asymetric)				
Cooling	Fanless				
Dimensional outline	772.0 × 230.0 × 563.5			mm	
Weight Net				Kg	
Weight Gross				Kg	
Control Type	Remote Control : Interfaced Type				
Screen Size	26",32",37",42",46"(16:9)				

3. A/V Circuit BLOCK Diagram

3.1 PC Mode

P C inputs, R, G, B , H, and V signals, are entered through D-Sub 15pin (DSUB1).
When PC is selected in MCU, the signals are entered into the SCALER, MST-6151DA (USC01).
MST6151DA is controlled using the MCU VCT49X3R(US02) Bus line of pin 41/42/43/47/48/49/50.
PC input resolution is Fh : 31~70k and Fv: 56~85Hz, and the maximum input resolution is 1360x768 at 60Hz.
Because MST6151DA Scaler has AD converter, data is operated RGB 24 bits.
If the resolution is above the specifications, an out of range message is displayed on the center of the screen.
However, even if the resolution is within the specified range, if the input timing is different from the timing indicated
on the manual, unsupported video, a message can be displayed.
The Geometry Adjust function, which is used to adjust the picture position and size, should be carried out in the Windows desktop screen,or full cross hatch.
The component signals, 480p, 720p, and 1080i, from the set-top box with a D-Sub out port, may be has not good image quality.

Sound L R signal of pc mode is entered pin117,118 of VCT49X3R. and sound processor is included in VCT49X3R.
Ouput Sound signal is outputted through pin 123,124 of MST6151DA ,and then this signal is entered audio amp YDA138E.
PC input and DVI input share a single audio jack

3.2 HDMI Mode

HDMI inputs (LVDS signal), 8bit, are entered through HDMI 19pin (CNG02). When HDMI is selected by MCU,
the LVDS signals are entered into digital port of the SCALER MST-6151DA (USC01).
MST6151DA is controlled using the MCU Bus line of pin 41/42/43/47/48/49/50.
the maximum resolution is 1360x768 at 65Hz. If the resolution is above the specifications, an out of range message
is displayed on the center of the screen. However, even if the resolution is within the specified range,
if the input timing is different from the timing indicated on the manual, unsupported video, a message can be displayed.

In hdmi mode, this model support 480p(60), 576p(50), 720p(50/60), 1080i(50/60) ,and pc timing on the manual.

3.3 COMPONENT Mode

Component signals Y, Pb(Cb),Pr(Cr) are entered port0 of mux PI5V330SWE(UC01).
mux PI5V330SWE is controlled by mcu.
When pin 1 of mux is low, component signal is outputted, and then Component signals

are entered into
The SCALER, MST-6151(USC01)DA.
The Component signals are composed of 480p (50/60Hz) for SD, 576p(60Hz),720p (50/60Hz) for HD, and 1080i (50/ 60Hz).

Component audio signal is entered audio mux TEA6422(UX01). Mux TEA6422 is controlled by SCL,SDA line of MCU VCT49X3R.

3.4 S-Video

S-Video signals are entered as Y/ C signals, which is composed of Luminance and color signals.
The PAL/SECAM are automatically detected by the video decoders VCT49X3R.
video decorder is included in VCT49X3R (US02).
Video signal is operated 656 format(8bit), and YUV 8bit signal is entered scaler video port.
S-Video input and composite video input share a single audio jack.
Therefore, while the pictures for the two inputs can be viewed at the same time, only one of the sounds can be heard.
S-video and composite audio signal is entered audio mux TEA6422(UX01).
Mux TEA6422 is controlled by SCL,SDA line of MCU VCT49X3R.

3.5 Video

Video signal is a composite signal that combines the Luminance (Y) and color (CHROMA) .
It is entered to the scaler IC, MST-6151DA (USC01).
Video signal is operated 656 format(8bit) as S-video , and YUV 8bit signal is entered scaler video port.

3.6 Scart Mode

Scart mode is separated full scart mode , half scart mode.
Full scart mode support CVBS video signal and RGB signal with audio signal.

half scart mode support CVBS video signal with audio signal.

Y-C Mode Signals is not Supported.

pin 8 high will auto select the SCART input. With a voltage range of 4.5V to 7.0V a compatible set will

select AV input in 16x9 mode. With a voltage range of 9.5v to 12.0v the set will select AV input in 4x3 mode.

pin 16 is used to select between composite or RGB input modes using the same SCART.
With a voltage of 1-3V DC (with respect to pin 18) RGBS input mode is selected.

With a voltage range of 0-0.4V composite mode is selected

3.7 IDTV Mode

DTV Y Pb Pr signal is inputted from digital board assy .

DTV signals Y, Pb(Cb),Pr(Cr) are entered port1 of mux PI5V330SWE(UC01).
mux PI5V330SWE is controlled by mcu.
When pin 1 of mux is high, dtv signal is outputted, and then dtv signals are entered into The SCALER, MST-6151(USC01)DA.
dtv signals are composed of 576i. dtv audio signal is entered audio mux TEA6422(UX01).
Mux TEA6422 is controlled by SCL,SDA line of MCU VCT49X3R.

3.8 Analog TV Mode

Rf signal from tuner(UX02) is generated IF. And IF signal is entered saw filter TFS96F(US01)

Output signal from saw filter is entered VCT49X3R. this signal is separated CVBS video and audio signal in VCT49X3R.

3.9 Supported PIP/POP Table

Sub\Main	PC	HDMI	iDTV	COMP	S-VIDEO	VIDEO	FScart	HScart	ANALOG TV
PC	X	X	X	X	O	O	O	O	O
HDMI	X	X	X	X	O	O	O	O	O
iDTV	X	X	X	X	O	O	O	O	O
COMP	X	X	X	X	O	O	O	O	O
S-VIDEO	O	O	O	O	X	X	X	X	X
VIDEO	O	O	O	O	X	X	X	X	X
FScart	O	O	O	O	X	X	X	X	X
HScart	O	O	O	O	X	X	X	X	X
ANALOG TV	O	O	O	O	X	X	X	X	X

X: Not supported, O: Supported

3.10 Scaler Output

Scaler output signals is R, G, B (each 8bits) LVDS signal .

This signal sent to the logic B/D in the LCD module.

3.11 Audio part

Audio input port for each mode:

Input	Port	Remark
PC /HDMI	RCA L/R 1EA	Shared
Scart	Scart Jack L/R	Full and half
CVBS /S-Video	RCA L /R 1EA	PAL
COMPONENT	RCA L /R 2EA	

Audio input signal for PC/HDMI,COMPONENT,S-VIDEO,SCART and CVBS modes is entered into the
audio processor IC(VCT49X3R), The audio processor (VCT49X3R) to control volume,
and left/right balance and mono/stereo and Sound effect.
The L/ R audio signal sent by VCT49X3R is amplified in the amplifier, YDA138E (UAU01),and sent to the speaker.
YDA138E Support 10W(based on impedance 8 ohm of output for L/R).

4. To use Service Mode

4.1 ENTERED INTO AGING MODE

1) REMOCON CONTROL
SET UP :MENU + S. MODE + SLEEP + MUTE Then go to number 5
Then go to number 3(Aging Option) ON
SET UP REMOVE :EXIT

4.2 CHECKING MCU VERSION

1) REMOCON CONTROL
- SET UP :MENU + S. MODE + SLEEP + MUTE Then You will see MCU VERSION
- GO TO Number 6

4. 3 FACTORY RESET

1) REMOCON CONTROL
- SET UP :MENU + S. MODE + SLEEP + MUTE Then go to number 7(FACTORY RESET)
- PRESS ENTER AND RIGHT KEY

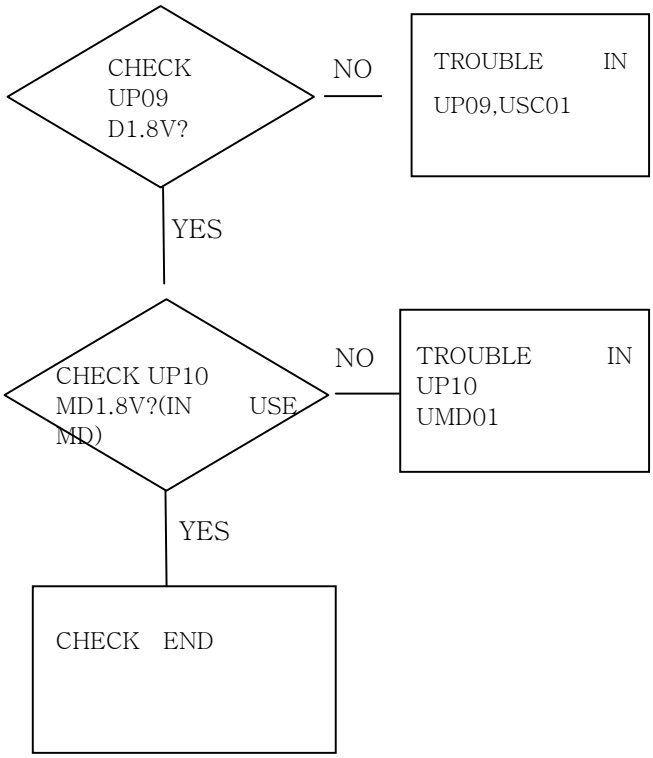
4**. 4 IN CASE DTV**

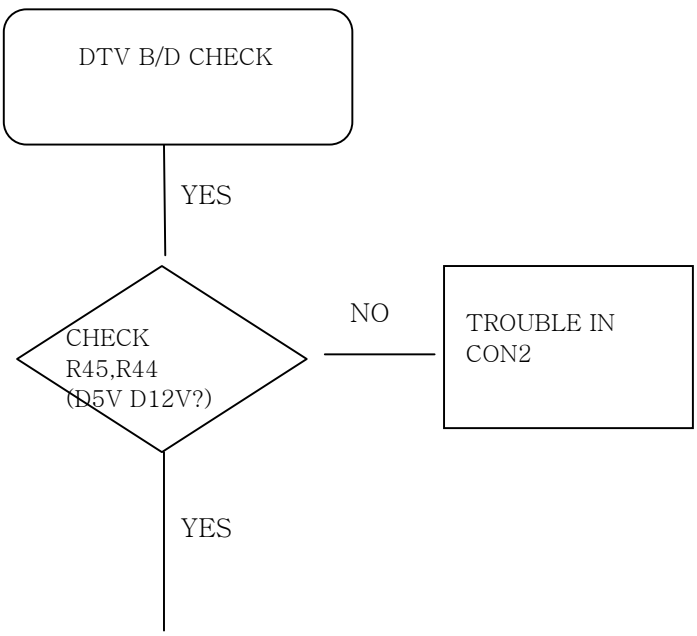
Go to DTV Source Then Press MENU and move DTV CHANNEL and move FACTORY SET and Press ENTER

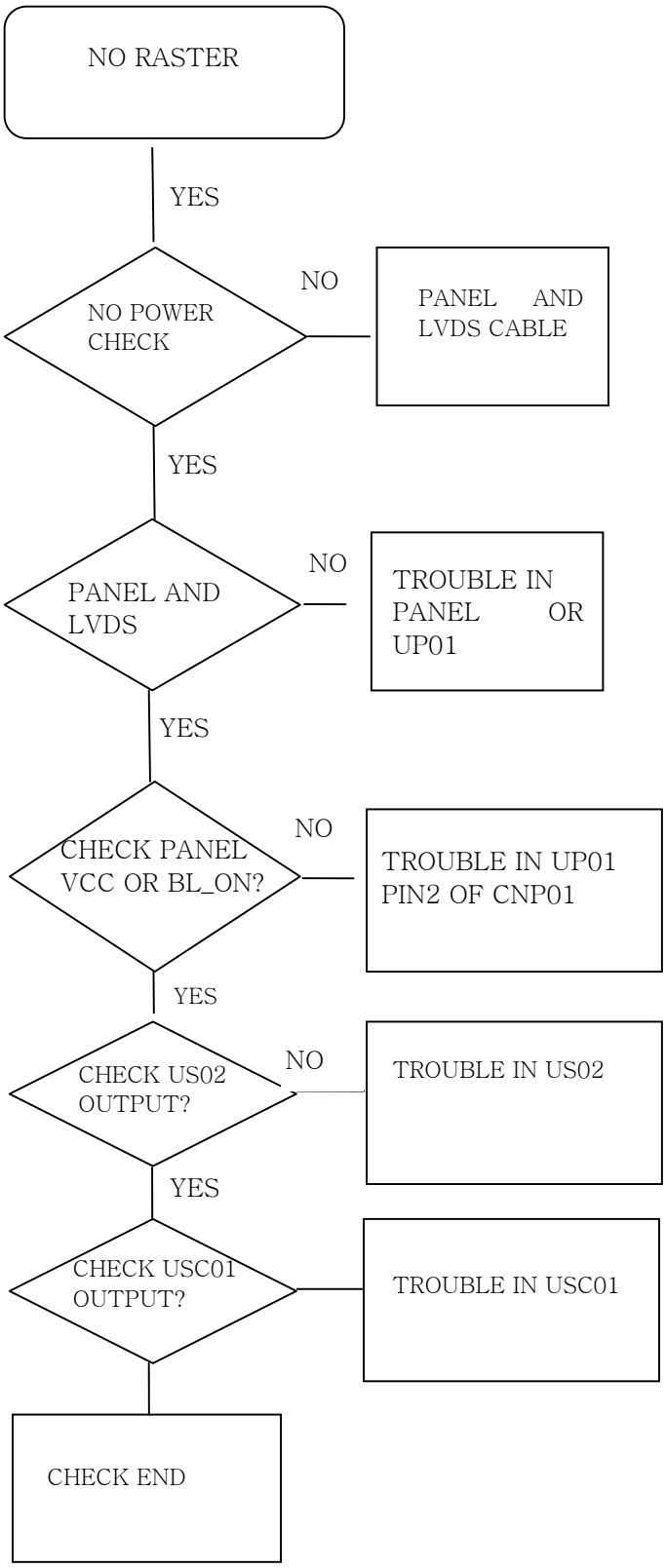
4.5. Exit Service menu

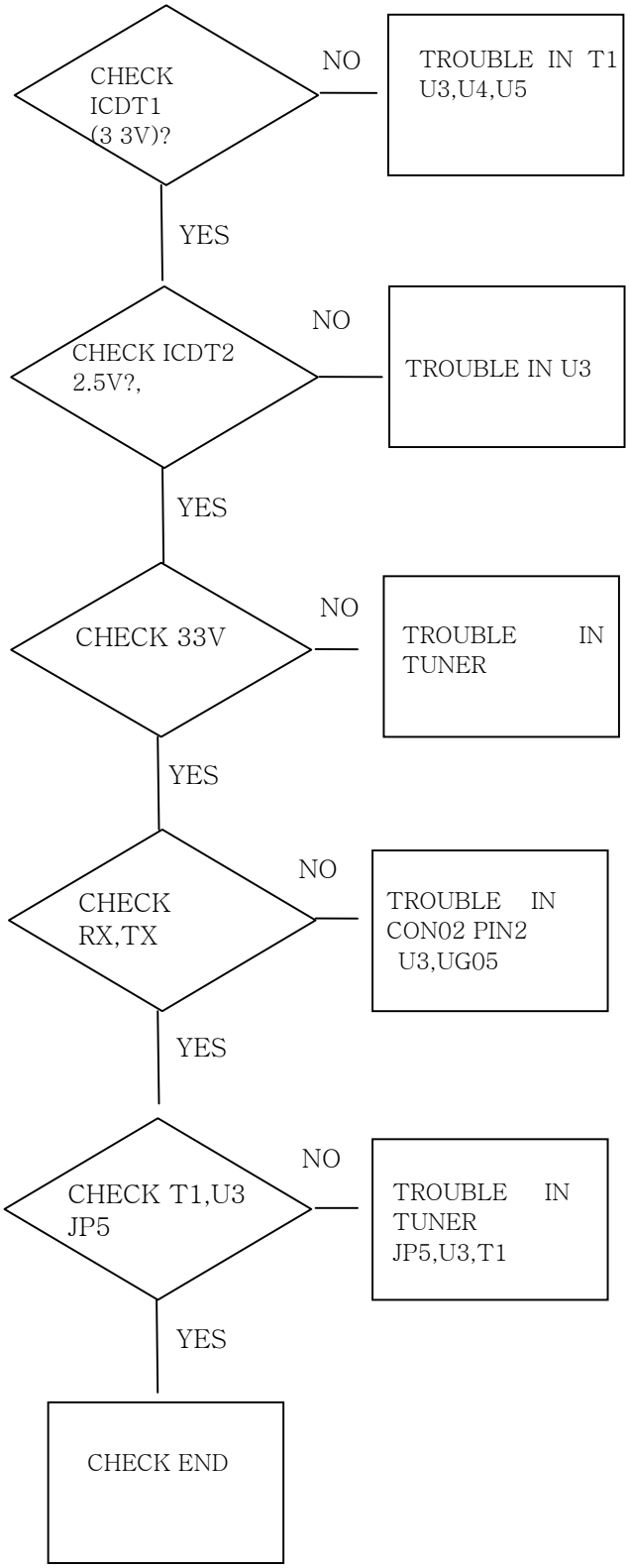
- press exit key

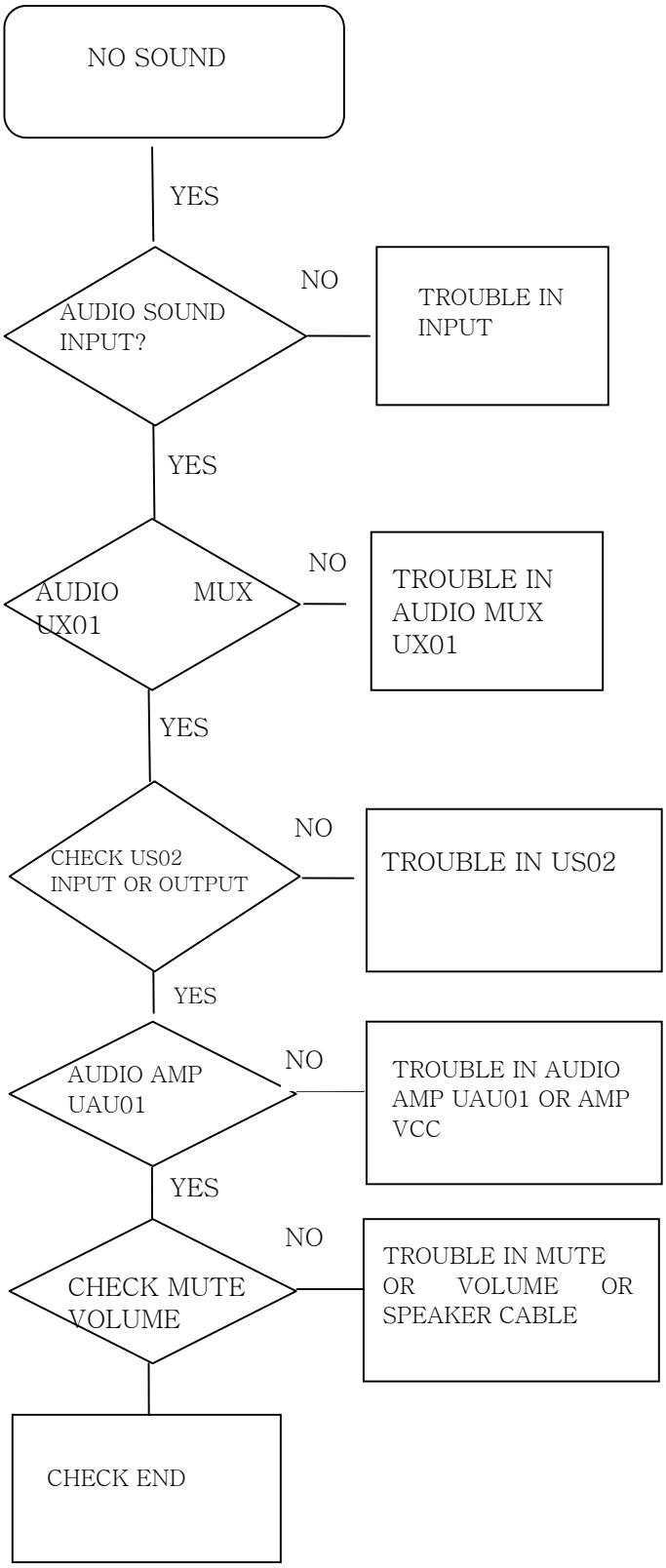
5.Trouble Shooting Guide


CHECK
UP09
D1.8V?
NO
TROUBLE IN
UP09,USC01
YES
CHECK UP10
MD1.8V?(IN USE
MD)
NO
TROUBLE IN
UP10
UMD01
YES
CHECK END


DTV B/D CHECK
YES
CHECK
R45,R44
(D5V D12V?)
NO
TROUBLE IN
CON2
YES


NO RASTER
YES
NO POWER CHECK
NO
PANEL AND LVDS CABLE
YES
PANEL AND LVDS
NO
TROUBLE IN PANEL OR UP01
YES
CHECK PANEL VCC OR BL_ON?
NO
TROUBLE IN UP01 PIN2 OF CNP01
YES
CHECK US02 OUTPUT?
NO
TROUBLE IN US02
YES
CHECK USC01 OUTPUT?
TROUBLE IN USC01
CHECK END


CHECK ICDT1 (3 3V)?
NO
TROUBLE IN T1 U3,U4,U5
YES
CHECK ICDT2 2.5V?,
NO
TROUBLE IN U3
YES
CHECK 33V
NO
TROUBLE IN TUNER
YES
CHECK RX,TX
NO
TROUBLE IN CON02 PIN2 U3,UG05
YES
CHECK T1,U3 JP5
NO
TROUBLE IN TUNER JP5,U3,T1
YES
CHECK END


NO SOUND
YES
AUDIO SOUND INPUT?
NO
TROUBLE IN INPUT
YES
AUDIO MUX UX01
NO
TROUBLE IN AUDIO MUX UX01
YES
CHECK US02 INPUT OR OUTPUT
NO
TROUBLE IN US02
YES
AUDIO AMP UAU01
NO
TROUBLE IN AUDIO AMP UAU01 OR AMP VCC
YES
CHECK MUTE VOLUME
NO
TROUBLE IN MUTE OR VOLUME OR SPEAKER CABLE
CHECK END

6. TV/ VIDEO System

<Digital>

6.1 Front –End(Tuner/Demodulator)

Input Frequency Range : VHF 174~230Mhz:ch5~ch12
230~470Mhz:ch71~ch99
UHF 470~860Mhz :ch21~ch69

RF Input(for aerial)connector	: female IEC 169-2
Channel bandwidth	German : 8Mhz/7Mhz (combine UHF/VHF)
	Others : 8Mhz (UHF only)
Input Impeadance	75ohms
OFDM Spectrum	2k and 8k carrier non hierarchical
Modulation Mode	16QAM,64QAM
Guard Interval Modes	1/32,1/16,1/8,1/4 active symbol duration
FEC Modes	Rate 1/2, 2/3, 3/4, 5/6, 7/8

6.2 Transport Demultiplexer

Demultiplexer	According to ISO/IEC 13818-1
Max.Input Stream	60Mbps(serial)/7.5Mbps(parallel)
PID Handling Capability	32PID
SI Filtering	According DVB-SI Spec.(ETS 300 468)

< Analog >

6.3 ATV STANDARD

- TV system :	PAL B/G, D/K, I, L, M
- RF signal :	VHF, UHF, CABLE TV
- Sound modulation:	AM/FM-Mono, FM-Stereo (A2, D/K), NICAM
- Color system :	PAL, SECAM

* APPLICATION

- Receiving System : (PAL STANDARD SYSTEM)
- Channel VHF : Low BAND : E2(48.25MHz) ~ S6(140.25MHz)
  High BAND : S7(147.25MHz) ~ S36(423.25MHz)
  UHF BAND : S37(431.25MHz) ~ C57(863.25MHz)
- Intermediate Frequency PIF : 38.9MHz (PAL B/G, I, D/K, SECAM L)
  33.9MHz (SECAM L')
  SIF : 33.4MHz (B/G), 32.9MHz(I), 32.4MHz(D/K)
  40.4MHz (SECAM L')

- Input Impedance : UHF/VHF Terminal (75) Ω, Unbalanced
- Band Change – Over System : (PLL Control System)
- Tuning System : (Electronic Tuning System With PLL)

6.4 Power Indicator LED

The LCD TV shall make use of an LED type indicator located on the front of the LCD TV.

The LED Color shall indicate the power states as follows.

* Power ON-LED is Green
* Power Off(Stand-by)- LED is Red(<1.8 watts)

6.5 Signal Input / Output specification

Parameter			Specification	Unit	Remarks
Speaker	Impedance		8(L) + 8(R)	Ω	
	Output		10	W	
Audio	Freq. Character		0.1 ~ 12	KHz	
	T.H.D		< 10	%	
	HUM		< 1	V	
	Output		10(L) + 10(R)	W	
Power Consumption	Max		125+10%	W	NOTE 1
	ST-BY		<2.0	W	
Composit Video Input			1	Vp-p	
Scart Input	Full	RGB	0.7	Vp-p	
		CVBS	1	Vp-p	
	Half	CVBS	1	Vp-p	
S- Video Input	Y		1	Vp-p	
	C		0.286	Vp-p	
Component Input	COMP	Y	1	Vp-p	1920 * 1080i 1280 * 720p 720 * 576p
		Pb	0.7	Vp-p	
		Pr	0.7	Vp-p	
	DTV	Y	1	Vp-p	720 * 576p
		Pb	0.7	Vp-p	
		Pr	0.7	Vp-p	
PC Input	RGB		0.7	Vp-p	VGA ~ XGA & HDTV (1080i, 720p, 576p)
	H Frequency		31 ~ 70(TTL Level)	KHz	
	V Frequency		56 ~ 85(TTL Level)	Hz	
Audio Input	L, R		0.5	Vrms	Mono or stereo
DVI Input	H Frequency		31 ~ 70(TTL Level)	KHz	
	V Frequency		60(TTL Level)	Hz	

VIDEO Out put	Composite		1.0	Vp-p	
Audio Output	L,R		0.5	Vrms	
Woofer out put	LOUD		0.5	Vrms	
Scart Output	Full	CVBS	1	Vp-p	
	Half	CVBS	1	Vp-p	

NOTE 1 .Power source : AC230V 50Hz
.It is measured on full screen white pattern

6.6 TV Input

* DEMOD. CHARACTERISTICS

NO.	ITEM		SPECIFICATIONS			UNIT	NOTES
			MIN.				
1-1	Video Output Level		2.0	2.3	2.6	Vp-p	* Input Level : 70dBuV * Video Signal : PAL(87.5%), SECAM (90%) AM Mod. STD Color Bar
1-2	Video Freq. Response 1 MHz 2 MHz 3 MHz 4 MHz 4.43 MHz		 -1.0 -1.5 -2.5 -3.0 -4.0	 -0.0 -0.0 -0.0 -0.0 -1.0	 +1.5 +2.0 +2.5 +3.0 +3.0	dB	* Input Level : 70dBuV * PALI: 87.5% AM Mod. * SECAM : 90% AM Mod. * FULL Sweepl * Reference : 0.5 MHZ
1-3	Luminance S/N Ratio		40	47	-	dB	* Input Level : VHF,UHF : 70dBuV * Setting of S/N Meter - HPF : 100KHz, - LPF : 5.0MHz * Video Signal : 87.5% AM Mod.100% White
1-4	NOISE LIMIT SENSITIVITY		-	43	51	dBuV	Video Signal : 100% White Sig. AT. S/N = 30dB
1-5	AFT ALIGNMENT ACCURACY		+50	0	-50	KHz	* Alignment Center : 1.9V * IF Input Level : 90dBuV * P/S : -10dB * Standard Color Bar : PAL(87.5%) SECAM L' (90%) * Center Frequency : PAL (38.9 MHz) SECAM L' (90%)
1-6	Chroma Distortion	DP	-10	5	10	DEG	* Input Level : 70dBuV * Video Signal: 87.5% AM Mod. RAMP Signal
		DG	-10	5	10	%	
1-7	BURST LEVEL		20.0	30	36	%	* Input Level : 70dBuV * Video Signal: 87.5% Mod. Standard Color Bar Sig.

1-8	SIF OUTPUT LEVEL		70	75		dBuV	* Input Level : 70dBuV * Video Signal: Standard Color Bar Sig. * CH : S20 * P/S Ratio : -10dB
1-9	AUDIO S/N RATIO		40	50		dB	* 1KHz ± 50KHz Dev. * Video Signal: 87.5% Mod. Standard Color Bar Sig. * Use CCITT FILTER
1-10	AUDIO DISTORTION RESPONSE		-	0.6	3.5	%	* 1KHz ± 50KHz Dev. * Standard Color Bar : 87.5% Mod. * De-emphasis ON
1-11	AUDIO FREQ. RES-PONSE	50Hz	- 3	0	+ 3	dB	* 50Hz ~ 10KHz * 1KHz ± 50KHz Dev *Standard Color Bar * De-emphasis ON
	10KHz	- 4	- 1				
1-12	AUDIO OUTPUT LEVEL		0.3	.06	.08	Vrms	* 1KHz ± 50KHz Dev * Standard Color Bar : 87.5% Mod.

6.7 Analog R.G.B Input (PC)

6.7.1 Timing

* Timing Chart
This monitor shall be capable of displaying following video timing chart.

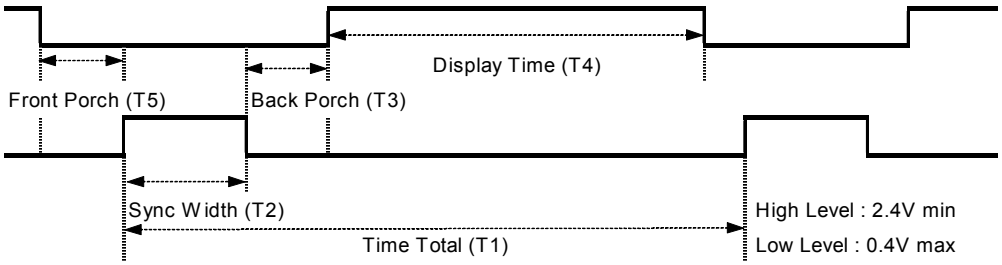


Fig. 3.2 - H-Sync

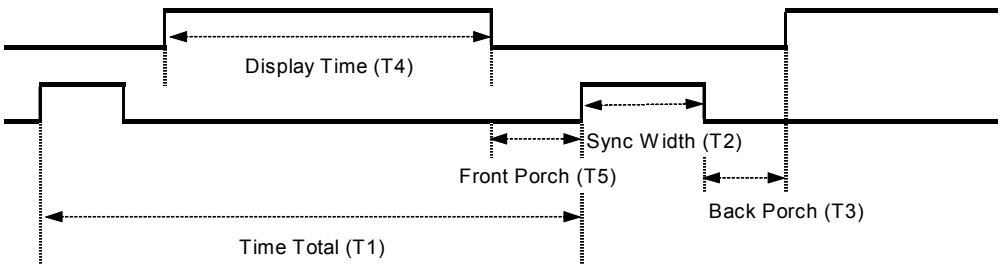


Fig. 3.3 - V-Sync

6.7.2 Preset-Mode Timing

The timing shown in the following table will be factory preset for display.

- preset mode table

Horizontal	Pixel	640	720	640	640	800	800	800	832	1024	1024	1024	1366	1280
Frequency	KHz	31.469	31.469	37.861	37.500	37.879	46.875	48.077	49.725	48.363	56.476	60.023	61.27	63.981
Period (T1)	μs	31.778	31.778	26.413	26.667	26.400	21.333	20.800	20.111	20.677	17.707	16.660	16.321	15.630
Sync Width (T2)	μs	3.813	3.813	1.270	2.032	3.200	1.616	2.400	1.117	2.092	1.813	1.219	0.451	1.037
Back Porch (T3)	μs	1.887	1.907	3.810	3.810	2.200	3.232	1.280	3.910	2.462	1.920	2.235	2.294	2.296
Active (T4)	μs	25.422	25.422	20.317	20.317	20.000	16.162	16.000	14.524	15.754	13.653	13.003	12.843	11.852
Front Porch (T5)	μs	0.636	0.636	0.508	0.508	1.000	0.323	1.120	0.559	0.369	0.320	0.203	0.734	0.445

Vertical	Lines	350	400	480	480	600	600	600	624	768	768	768	768	1024
Frequency	Hz	70	70.080	72.809	75.000	60.316	75.000	72.188	74.550	60.004	70.069	75.029	74.994	60.020
Period (T1)	ms	14.268	14.268	13.735	13.333	16.579	13.333	13.853	13.414	16.666	14.272	13.328	13.334	16.661
Sync Width (T2)	ms	0.064	0.064	0.079	0.080	0.106	0.064	0.125	0.060	0.124	0.106	0.050	0.082	0.047
Back Porch (T3)	ms	1.906	1.080	0.528	0.427	0.607	0.448	0.478	0.784	0.600	0.513	0.466	0.506	0.594
Active (T4)	ms	11.122	12.711	12.678	12.800	15.840	12.800	12.480	12.549	15.880	13.599	12.795	12.535	16.005
Front Porch (T5)	ms	1.176	0.413	0.026	0.027	0.026	0.021	0.770	0.021	0.062	0.053	0.017	0.212	0.015
Interlaced	Y/N	N	N	N	N	N	N	N	N	N	N	N	N	N
Sync Polar	H	+	−	−	−	+	+	+	+	−	−	+	+	+
	V	−	+	−	−	+	+	+	+	−	−	+	+	+

7. Input connector Characteristics

7.1 PC connector cable

The Pin assignments shall be listed as below.

PIN No.	Assignment
1	Red
2	Green
3	Blue
4	GND
5	GND
6	Red GND
7	Green GND
8	Blue GND
9	BLANK
10	SYNC GND
11	GND
12	SDA
13	H-SYNC
14	V-SYNC
15	SCL

- Video signals on 75 ohm termination to the ground

  Red, Green & Blue Video (refer to Fig.3.1)

  Level : 0 to 0.7 Vp-p Polarity : Positive

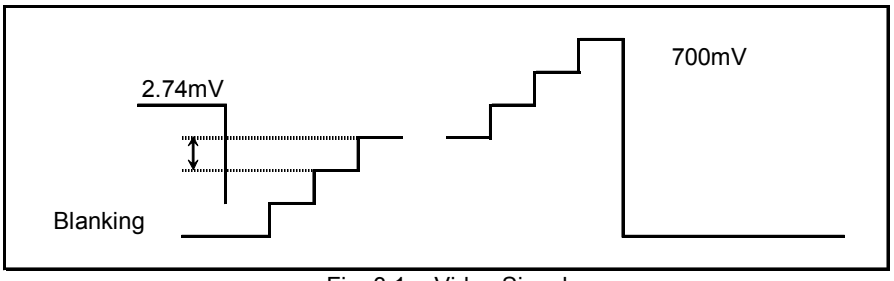
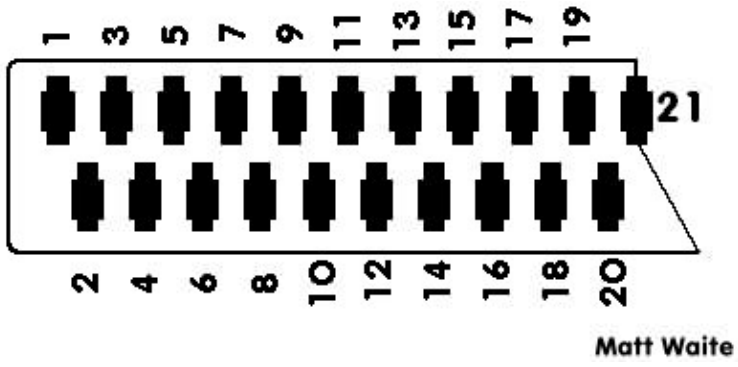


Fig. 3.1 - Video Signal

7.2 SCART (EURO) Connector

Pin number	Description	Video
1	Right audio out (500mV rms Lo Z)	

2	Right audio in (500mV rms Hi Z)	
3	Left audio out (500mV rms Lo Z)	
4	Audio ground	
5	Blue video ground	GND
6	Left audio in (500mV rms Hi Z)	
7	Blue video in (700mV p-p 75R)	INPUT
8	Source switching / 16x9 [note 1]	
9	Green video ground	GND
10	Data bus	
11	Green video in (700mV p-p 75R)	INPUT
12	Data bus	
13	Red video ground	GND
14	Data bus ground	
15	Red video in (700mV p-p 75R)	C IN / IN
16	Fast blanking (<0.5V off , >1V on) [note 2]	
17	Composite video ground	GND
18	Fast blanking ground	
19	Composite video out (1V inc syncs)	OUTPUT
20	Composite video in (1V inc syncs)	Y IN / IN
21	Chassis ground	



(pictured looking at solder side of plug)

Note 1: (Pin 8 usage)
On many TV's taking pin 8 high will auto select the SCART input. With a voltage range of 4.5V to 7.0V

a compatible set will select AV input in 16x9 mode. With a voltage range of 9.5v to 12.0v

the set will select AV input in 4x3 mode.

It has come to my attention that certain newer sets (notably those containing Sony CXA2069A chipset)

implement a third intermediate switching level. Details are sketchy,

but it would appear to select a letterbox format rather than full 4:3 or full 16:9.

Note 2 : (Pin 16 usage)
On some devices pin 16 is used to select between composite or RGB input modes using the same SCART.
With a voltage of 1-3V DC (with respect to pin 18) RGBS input mode is selected.

The switching signal needs to be able to source upto 20mA.

With a voltage range of 0-0.4V composite mode is selected

Scart supports CVBS Signals , RGB(Full-Scart) and Audio Right Left ,

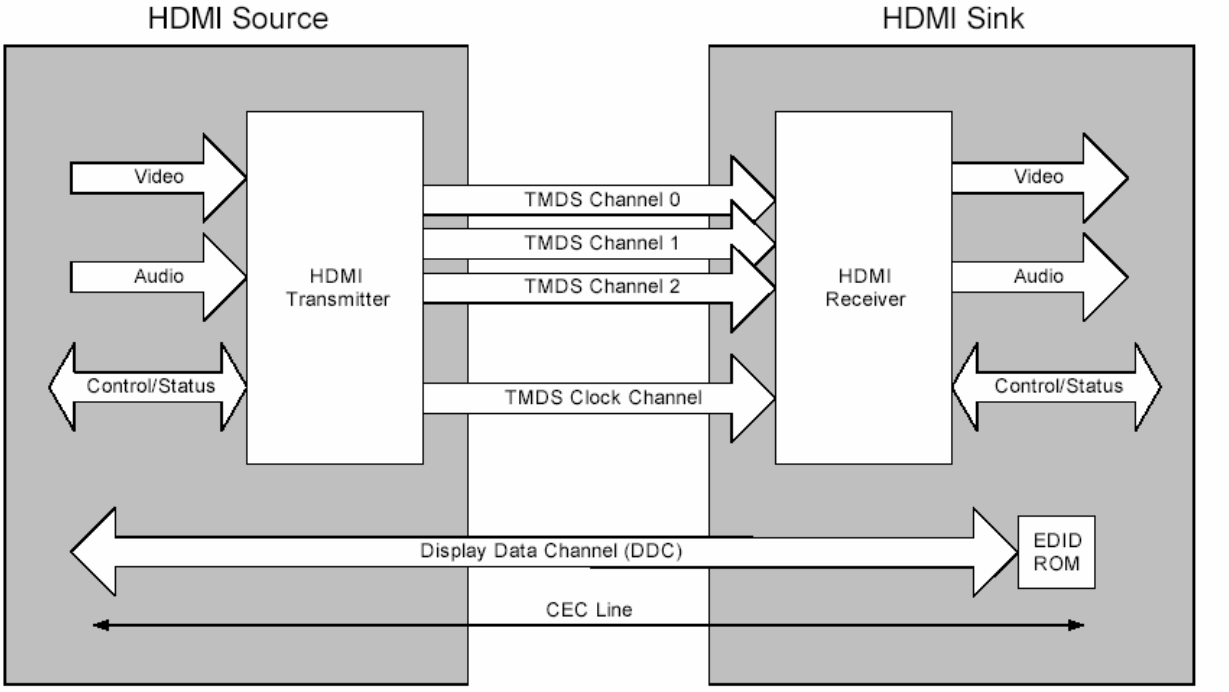
and Y-C Mode Signals is not Supported.

7.3 HDMI (High-Definition Multimedia Interface)

7.3.1 Overview

-HDMI system architecture is defined to consist of Sources and Sinks.
A given device may have one or more HDMI inputs and one or more HDMI outputs.
Each HDMI input on these devices shall follow all of the rules for an HDMI Sink
and each HDMI output shall follow all of the rules for an HDMI Source.

- As shown in ***Figure 12-1 HDMI Block Diagram*** the HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio and auxiliary data. In addition, HDMI carries a VESA DDC channel. The DDC is used for configuration and status exchange between a single Source and a single Sink.
The optional CEC protocol provides high-level control functions between all of the various audiovisual products in a user's environment.



12-1 HDMI Block Diagram

- Audio, video and auxiliary data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver as a frequency reference for data recovery on the three TMDS data channels.

- Video data is carried as a series of 24-bit pixels on the three TMDS data channels. TMDS encoding converts the 8 bits per channel into the 10 bit DC-balanced, transition minimized sequence which is then transmitted serially across the pair at a rate of 10 bits per pixel clock period.

- Video pixel rates can range from 25MHz to 165MHz. Video formats with rates below 25MHz can be transmitted using a pixel-repetition scheme. The video pixels can be encoded in either RGB, YC_BC_R 4:4:4 or YC_BC_R 4:2:2 formats. In all three cases, up to 24 bits per pixel can be transferred.

- Basic audio functionality consists of a single IEC 60958 audio stream at sample rates of 32kHz, 44.1kHz or 48kHz. This can accommodate any normal stereo stream. Optionally, HDMI can carry a single such

stream at sample rates up to 192KHz or from two to four such streams (3 to 8 audio channels) at sample
rates up to 96KHz. HDMI can also carry IEC 61937 compressed (e.g. surround-sound) stream at sample
rates up to 192kHz.

- The DDC is used by the Source to read the Sink's Enhanced Extended Display Identification Data
(E-EDID) in order to discover the Sink.s configuration and/or capabilities.

7.3.2 Connectors and Cables

- A device.s external HDMI connection shall be presented via one of the two specified HDMI connectors,
Type A or Type B. This connector can be attached directly to the device or can be attached via a cable
adapter that is shipped with the device.

- The Type A connector carries all required HDMI signals, including a single TMDS link. The Type B
connector is slightly larger and carries a second TMDS link, which is necessary to support very high-
resolution computer displays requiring dual link bandwidth. A passive cable adapter between Type A and
Type B connectors is specified.

7.3.3 Connectors Pin Assignment

PIN	Signal Assignment	PIN	Signal Assignment
1	TMDS Data2+	2	TMDS Data2 Shield
3	TMDS Data2–	4	TMDS Data1+
5	TMDS Data1 Shield	6	TMDS Data1–
7	TMDS Data0+	8	TMDS Data0 Shield
9	TMDS Data0–	10	TMDS Clock+
11	TMDS Clock Shield	12	TMDS Clock–
13	CEC	14	Reserved (N.C. on device)
15	SCL	16	SDA
17	DDC/CEC Ground	18	+5V Power
19	Hot Plug Detect		

Type A connector Pin Assingment

AMS1085

Advanced Monolithic Systems

AMS1085

3A LOW DROPOUT VOLTAGE REGULATOR

FEATURES

- **Three Terminal Adjustable or Fixed Voltages 1.5V, 2.5V, 2.85V, 3.0V, 3.3V, 3.5V and 5.0V**
- **Output Current of 3A**
- **Operates Down to 1V Dropout**
- **Load Regulation: 0.1%**
- **Line Regulation: 0.015%**
- **TO-220, TO-263 and TO-252 packages available**

APPLICATIONS

- **High Efficiency Linear Regulators**
- **Post Regulators for Switching Supplies**
- **Microprocessor Supply**
- **Battery Chargers**
- **Constant Current Regulators**
- **Notebook/Personal Computer Supplies**
- **Portable Instrumentation**

GENERAL DESCRIPTION

The AMS1085 series of adjustable and fixed voltage regulators are designed to provide 3A output current and to operate down to 1V input-to-output differential. The dropout voltage of the device is guaranteed maximum 1.5V at maximum output current, decreasing at lower load currents.

On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress under overload conditions on both the regulator and power source circuitry.

The AMS1085 devices are pin compatible with older three-terminal regulators and are offered in 3 lead TO-220 package, 3 and 2 lead TO-263 (Plastic DD) and TO-252 (D PAK) package.

ORDERING INFORMATION:

PACKAGE TYPE			OPERATING JUNCTION TEMPERATURE RANGE
3 LEAD TO-220	2&3 LEAD TO-263	TO-252	
AMS1085CT	AMS1085CM	AMS1085CD	0 to 125° C
AMS1085CT-1.5	AMS1085CM-1.5	AMS1085CD-1.5	0 to 125° C
AMS1085CT-2.5	AMS1085CM-2.5	AMS1085CD-2.5	0 to 125° C
AMS1085CT-2.85	AMS1085CM-2.85	AMS1085CD-2.85	0 to 125° C
AMS1085CT-3.0	AMS1085CM-3.0	AMS1085CD-3.0	0 to 125° C
AMS1085CT-3.3	AMS1085CM-3.3	AMS1085CD-3.3	0 to 125° C
AMS1085CT-3.5	AMS1085CM-3.5	AMS1085CD-3.5	0 to 125° C
AMS1085CT-5.0	AMS1085CM-5.0	AMS1085CD-5.0	0 to 125° C

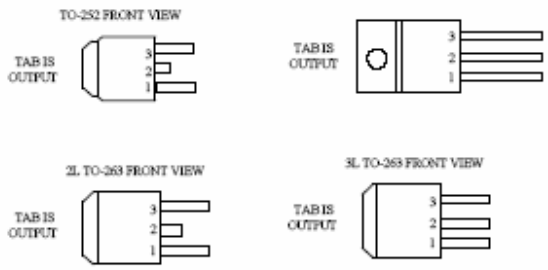
PIN CONNECTIONS

FIXED VERSION

1- Ground
2- V_{OUT}
3- V_{IN}

ADJUSTABLE VERSION

1- Adjust
2- V_{OUT}
3- V_{IN}



Advanced Monolithic Systems, Inc. www.advanced-monolithic.com Phone (925) 443-0722 Fax (925) 443-0723

ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation	Internally limited
Input Voltage	15V
Operating Junction Temperature	
Control Section	0°C to 125°C
Power Transistor	0°C to 150°C
Storage temperature	- 65°C to +150°C

Soldering information	
Lead Temperature (10 sec)	300°C
Thermal Resistance	
TO-220 package	φ_{JA}= 50°C/W
TO-263 package	φ_{JA}= 30°C/W *
TO-252 package	φ_{JA}= 100°C/W

* With package soldering to 0.5in^2 copper area over backside ground plane or internal power plane φ_{JA} can vary from 20°C/W to >40°C/W depending on mounting technique.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics at I_{OUT} = 0 mA, and T_J = +25°C unless otherwise specified.

Parameter	Device	Conditions	Min	Typ	Max	Units
Reference Voltage (Note 2)	AMS1085	I_{OUT} = 10 mA 10mA ≤ I_{OUT} ≤ 3A, 1.5V≤ (V_{IN} - V_{OUT}) ≤ 12V	1.238 **1.225**	1.250 **1.250**	1.262 **1.270**	V V
Output Voltage (Note 2)	AMS1085-1.5	0 ≤ I_{OUT} ≤ 3A , 3V≤ V_{IN} ≤ 12V	1.485 **1.470**	1.500 **1.500**	1.515 **1.530**	V V
	AMS1085-2.5	0 ≤ I_{OUT} ≤ 3A , 4V≤ V_{IN} ≤ 12V	2.475 **2.450**	2.500 **2.500**	2.525 **2.550**	V V
	AMS1085-2.85	0 ≤ I_{OUT} ≤ 3A , 4.35V≤ V_{IN} ≤ 12V	2.82 **2.79**	2.850 **2.850**	2.88 **2.91**	V
	AMS1085-3.0	0 ≤ I_{OUT} ≤ 3A , 4.5V ≤ V_{IN} ≤ 12V	2.970 **2.940**	3.000 **3.000**	3.300 **3.360**	V V
	AMS1085-3.3	0 ≤ I_{OUT} ≤ 3A , 4.75V ≤ V_{IN} ≤ 12V	3.267 **3.235**	3.300 **3.300**	3.333 **3.365**	V V
	AMS1085-3.5	0 ≤ I_{OUT} ≤ 3A , 5V ≤ V_{IN} ≤ 12V	3.465 **3.430**	3.500 **3.500**	3.535 **3.570**	V V
	AMS1085-5.0	0 ≤ I_{OUT} ≤ 3A , 6.5V ≤ V_{IN} ≤ 12V	4.950 **4.900**	5.000 **5.000**	5.050 **5.100**	V V
Line Regulation	AMS1085/-1.5/-2.5/-2.85/ -3.0/-3.3/-3.5/-5.0	I_{LOAD} = 10 mA , 1.5V≤ (V_{IN} - V_{OUT}) ≤ 12V		0.3 **0.6**	10 **10**	mV mV
Load Regulation (Notes 2, 3)	AMS1085	(V_{IN} - V_{OUT}) =3V, 10mA ≤ I_{OUT} ≤ 3A		0.1 **0.2**	.03 **.04**	% %
	AMS1085-1.5	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 3A		3 **6**	12 **20**	mV mV
	AMS1085-2.5	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 3A		3 **6**	12 **20**	mV mV
	AMS1085-2.85	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 3A		3 **6**	12 **20**	mV mV
	AMS1085-3.0	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 3A		3 **6**	12 **20**	mV mV
	AMS1085-3.3	V_{IN} = 5V, 0 ≤ I_{OUT} ≤ 3A		3 **7**	15 **25**	mV mV
	AMS1085-3.5	V_{IN} = 5.25V, 0 ≤ I_{OUT} ≤ 3A		3 **6**	15 **25**	mV mV
	AMS1085-5.0	V_{IN} = 8V, 0 ≤ I_{OUT} ≤ 3A		5 **10**	20 **35**	mV mV
Dropout Voltage (V_{IN} - V_{OUT})	AMS1085/-1.5/-2.5/-2.85/ -3.0/-3.3/-3.5/-5.0	ΔV_{OUT}, ΔV_{REF} = 1%, I_{OUT} = 3 A (Note 4)		**1.3**	**1.5**	V

PERICOM®

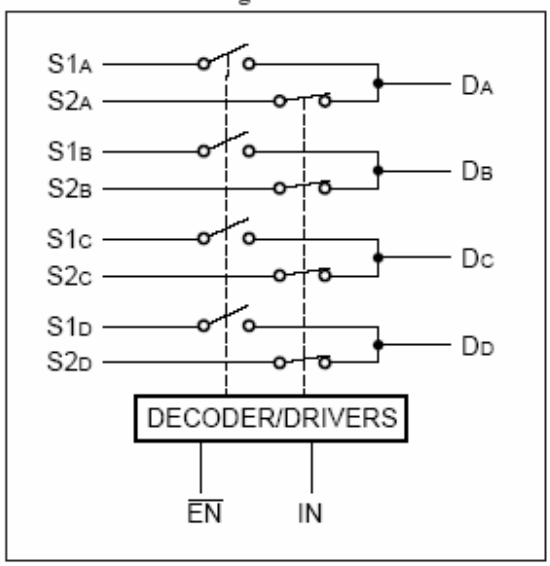
PI5V330

Low ON-Resistance Wideband/Video Quad 2-Channel MUX/DEMUX

Product Features:

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: –58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
  - 16-pin 300-mil wide plastic SOIC (S)
  - 16-pin 150-mil wide plastic SOIC (W)
  - 16-pin 150-mil wide plastic QSOP (Q)

Functional Block Diagram



Truth Table

$\overline{EN}$	IN	ON Switch
0	0	S1A, S1B, S1C, S1D
0	1	S2A, S2B, S2C, S2D
1	X	Disabled

Product Description:

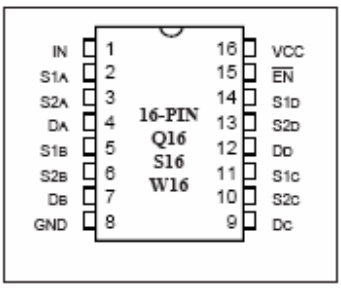
Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16-Pin Product Configuration



Product Pin Description

Pin Name	Description
S1A, S2A S1B, S2B S1C, S2C S1D, S2D	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
DA, DB, DC, DD	Analog Video I/O
GND	Ground
VCC	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ±5%)

Parameters	Description	Test Conditions[1]	Min.	Typ[2]	Max.	Units
V_{ANALOG}	Analog Signal Range		0	—	2.0	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	–0.5	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND	—	—	±1	µA
I_O	Analog Output Leakage Current	0≤S1, S2 or D≤V_{CC}, Switch Off	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA	—	–0.7	–1.2	V
I_{OS}	Short Circuit Current[3]	S1, S2, D = 0V V_{CC}	100	—	—	mA
V_H	Input Hysteresis at Control Pins		—	150	—	mV
R_{ON}	Switch On Resistance[4]	V_{CC} = Min., V_{IN} = 1.0V R_L = 75ohm, I_{ON} = 13 mA	—	3	7	ohm
		V_{CC} = Min., V_{IN} = 2.0V R_L = 75ohm, I_{ON} = 26 mA	—	7	10	ohm

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Measured by the voltage drop between S1, S2, and D I/O pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the S1, S2, and D I/O pins.

AK4386

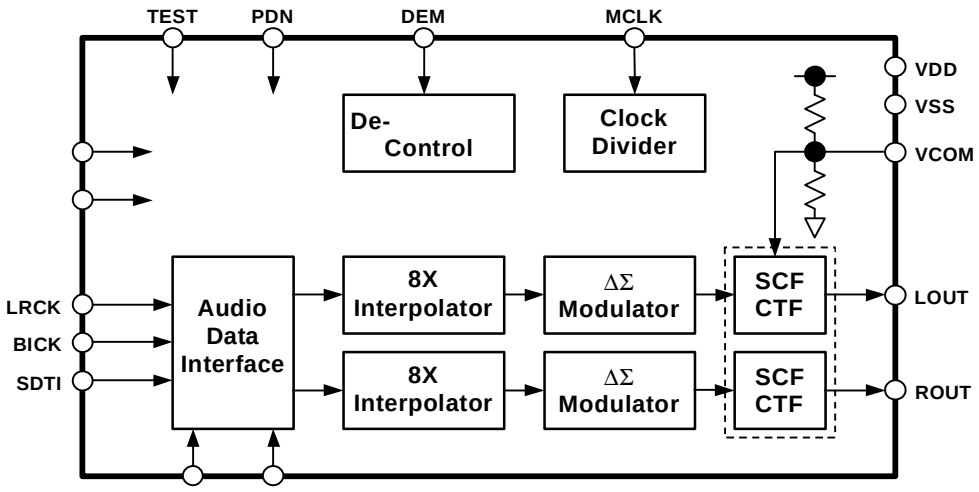
100dB 96kHz 24-Bit 2ch ΔΣ

GENERAL DESCRIPTION

The AK4386 is a 24bit low voltage & low power stereo DAC. The AK4386 uses the Advanced Multi-Bit ΔΣ architecture, this architecture achieves DR=100dB at 3V operation. The AK4386 integrates a combination of SCF and CTF filters increasing performance for systems with excessive clock jitter. The AK4386 is suitable for the portable audio system like MP3 and the home audio systems like STB and TV, etc as low power and small package. The AK4386 is offered in a space saving 16pin TSSOP package.

FEATURES

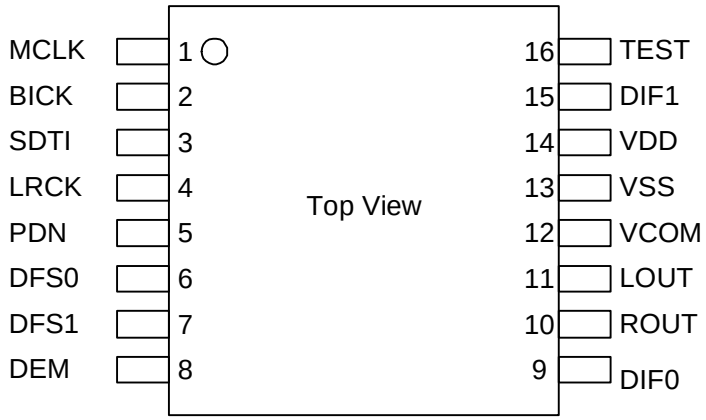
- ☐ **Sampling Rate: 8kHz ~ 96kHz**
- ☐ **24-Bit 8 times FIR Digital Filter**
- ☐ **SCF with high tolerance to clock jitter**
- ☐ **Single-ended output buffer**
- ☐ **Digital de-emphasis for 44.1kHz sampling**
- ☐ **I/F Format: 24-Bit MSB justified, 16/24-Bit LSB justified, I^2S Compatible**
- ☐ **Master Clock:**
  - **512/768/1024/1536fs for Half Speed (8kHz ~ 24kHz)**
  - **256/384/512/768fs for Normal Speed (8kHz ~ 48kHz)**
  - **128/192/256/384fs for Double Speed (48kHz ~ 96kHz)**
- ☐ **CMOS Input Level**
- ☐ **THD+N: –86dB**
- ☐ **DR, S/N: 100dB(@VDD=3.0V)**
- ☐ **Power Supply: 2.2 to 3.6V**
- ☐ **Ta = –40 ~ 85°C**
- ☐ **16pin TSSOP**



■ Ordering Guide

AK4386VT	−40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4386	Evaluation Board for AK4386	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	Input Channel Clock Pin
5	PDN	I	Full Power Down Mode Pin "L" : Power down, "H" : Power up
6	DFS0	I	Sampling Speed Select 0 Pin
7	DFS1	I	Sampling Speed Select 1 Pin
8	DEM	I	De-emphasis Filter Enable Pin "L" : OFF, "H" : ON (De-emphasis of fs=44.1kHz is enable.)
9	DIF0	I	Audio Interface Format 0 Pin
10	ROUT	O	Rch Analog Output Pin
11	LOUT	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Output Pin, 0.55 × VDD Normally connected to VSS with a 4.7μF (min. 1μF, max. 10μF) electrolytic capacitor.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin, 2.2 ~ 3.6V
15	DIF1	I	Audio Interface Format 1 Pin
16	TEST	I	TEST Pin This pin should be connected to VDD.

Note: All digital input pins should not be left floating.

■ Handling of Unused Pin

The unused output pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT, ROUT	This pin should be open.

DESCRIPTION

The Hynix HY5DU281622ET is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the point-to-point applications which require high densities and high bandwidth.

The Hynix 8Mx16 DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

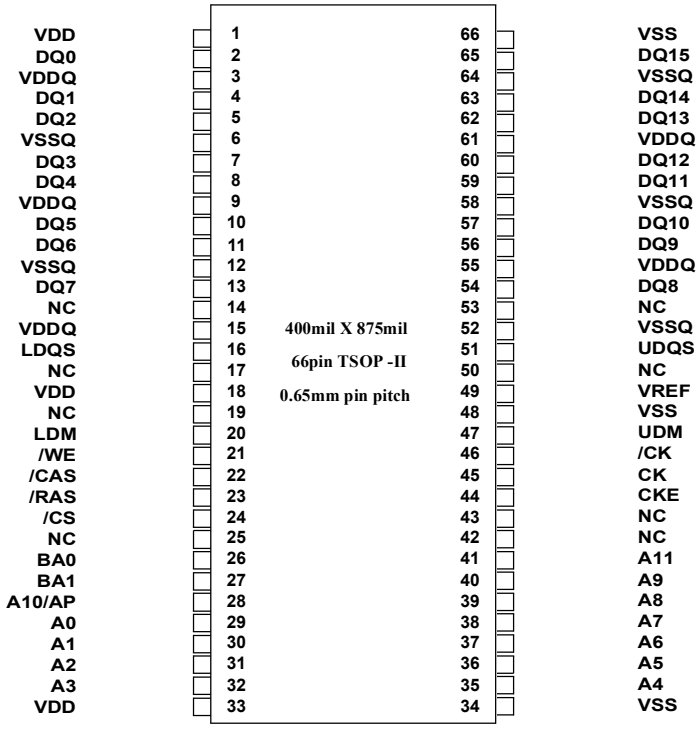
FEATURES

- 2.8V +/- 0.1V V_{DD} and V_{DDQ} power supply supports 400/375/350/333/300MHz
- 2.5V +/- 5% V_{DD} and V_{DDQ} power supply supports 275/250/200/166MHz
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC Standard 400 mil x 875 mil 66 Pin TSOP II, with 0.65mm pin pitch
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (UDQS,LDQS)
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Data(DQ) and Write masks(DM) latched on the both rising and falling edges of the data strobe
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Write mask byte controls by DM (UDM,LDM)
- Programmable /CAS Latency 5, 4 and 3 are supported
- Programmable Burst Length 2, 4 and 8 with both sequential and interleave mode
- Internal 4 bank operation with single pulsed /RAS
- tRAS Lock-Out function are supported
- Auto refresh and self refresh are supported
- 4096 refresh cycles / 32ms
- Full strength, Half strength and Weak Impedance driver options controlled by EMRS

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Max Data Rate	interface	Package
HY5DU281622ET-25	VDD/VDDQ=2.8V	400MHz	800Mbps/pin	SSTL_2	400 x 875mil ^{2} 66 Pin TSOP II
HY5DU281622ET-26		375MHz	750Mbps/pin		
HY5DU281622ET-28		350MHz	700Mbps/pin		
HY5DU281622ET-30		333MHz	666Mbps/pin		
HY5DU281622ET-33		300MHz	600Mbps/pin		
HY5DU281622ET-36	VDD/VDDQ=2.5V	275MHz	550Mbps/pin		
HY5DU281622ET-4		250MHz	500Mbps/pin		
HY5DU281622ET-5		200MHz	400Mbps/pin		

PIN CONFIGURATION (Top View)



ROW AND COLUMN ADDRESS TABLE

ITEMS	8Mx16
Organization	2M x 16 x 4banks
Row Address	A0 - A11
Column Address	A0-A8
Bank Address	BA0, BA1
Auto Precharge Flag	A10
Refresh	4K

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry and exit. CKE is asynchronous for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
UDM, LDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15
UDQS, LDQS	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15
DQ0 ~ DQ15	I/O	Data input / output pin : Data Bus
V_{DD}/V_{SS}	Supply	Power supply for internal circuits and input buffers.
V_{DDQ}/V_{SSQ}	Supply	Power supply for output buffers for noise immunity.
V_{REF}	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

K4S643232H

SDRAM 64Mb H-die (x32) CMOS SDRAM

512K x 32Bit x 4 Banks

FEATURES

? JEDEC standard 3.3V power supply
? LVTTL compatible with multiplexed address
? Four banks operation
? MRS cycle with address key programs
  -. CAS latency (2 & 3)
  -. Burst length (1, 2, 4, 8 & Full page)
  -. Burst type (Sequential & Interleave)
? All inputs are sampled at the positive going edge of the system clock.
? Burst read single-bit write operation
? DQM (x4,x8) & L(U)DQM (x16) for masking
? Auto & self refresh
? 15.6us refresh duty cycle

GENERAL DESCRIPTION

The K4S643232H is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

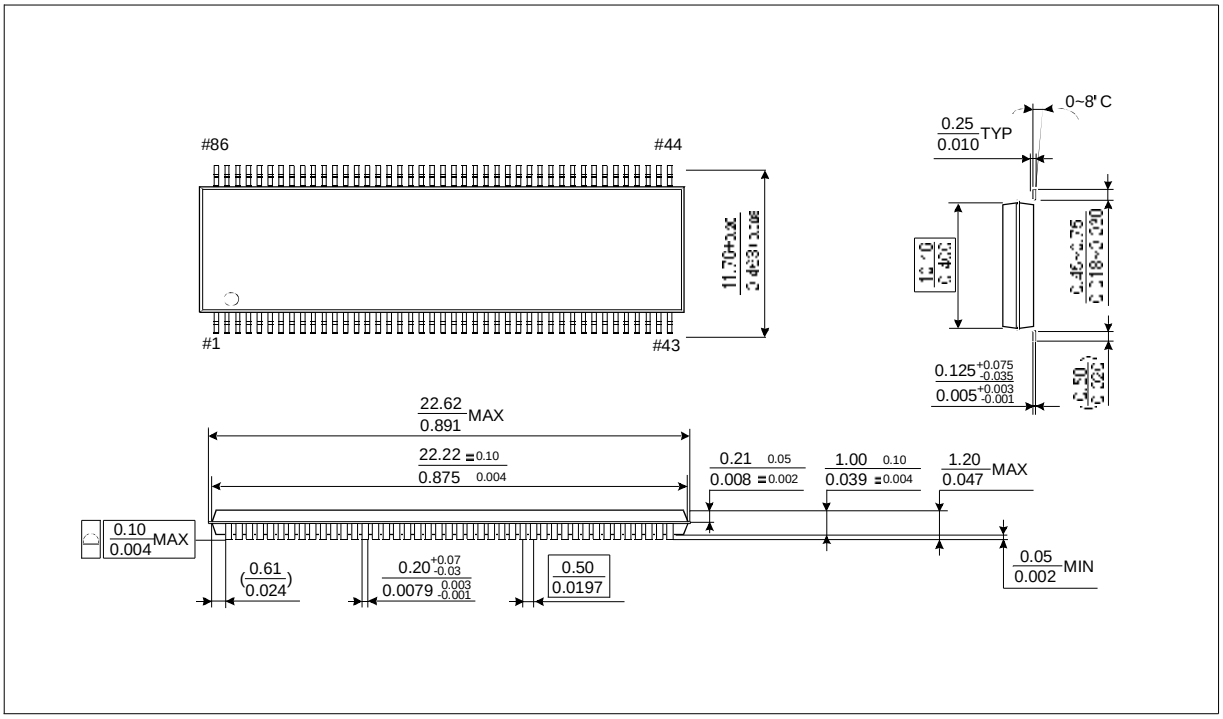
Ordering Information

Part No.	Orgainization	Max Freq.	Interface	Package
K4S643232H-TC/L70	512K x 32	143MHz	LVTTL	86pin TSOP
K4S643232H-TC/L60	512K x 32	166MHz	LVTTL	86pin TSOP
K4S643232H-TC/L55	512K x 32	183MHz	LVTTL	86pin TSOP
K4S643232H-TC/L50	512K x 32	200MHz	LVTTL	86pin TSOP

Organization	Row Address	Column Address
1Mx32	A0~A10	A0-A7

Row & Column address configuration

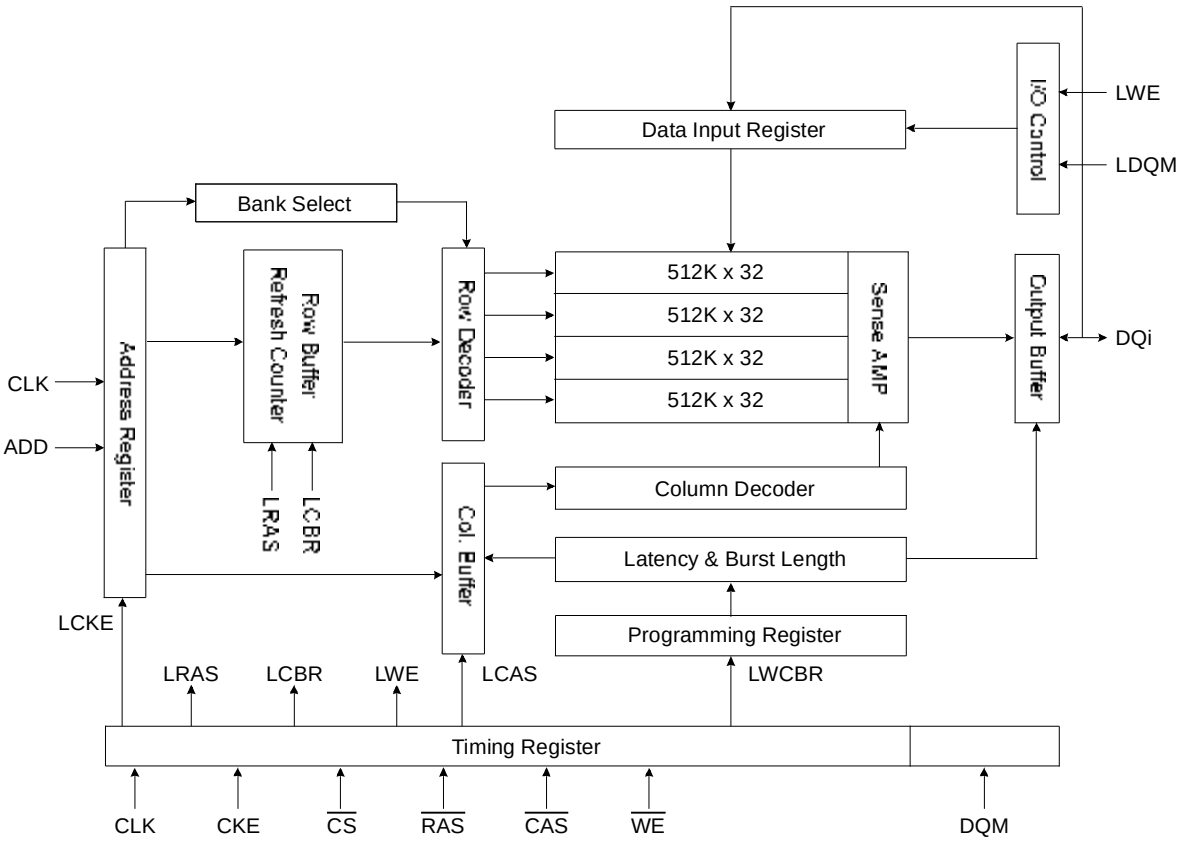
Package Physical Dimension



86Pin TSOP Package Dimension

SDRAM 64Mb H-die (x32) CMOS SDRAM

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down mode.
A_0 ~ A_{10}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_7
BA0,1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 3	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim 31}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	*No Connection*	This pin is recommended to be left No connection on the device.

K6X4008T1F

K6X4008T1F Family CMOS SRAM

512K×8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 512K×8
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 32-SOP-525, 32-TSOP2-400F/R
  32-TSOP1-0813.4F

GENERAL DESCRIPTION

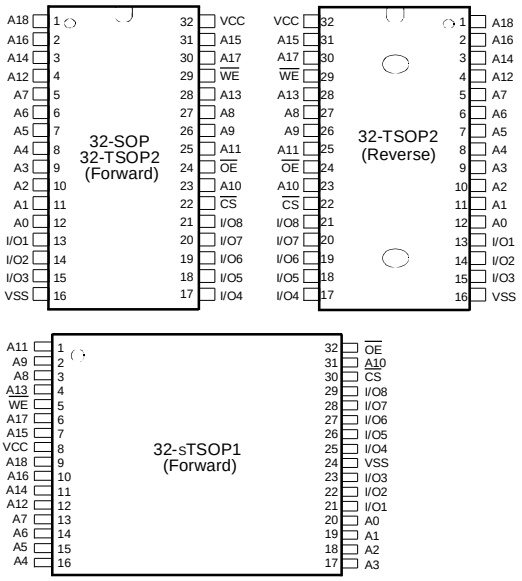
The K6X4008T1F families are fabricated by SAMSUNG′s advanced full CMOS process technology. The families support various operating temperature range and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
K6X4008T1F-B	Commercial(0~70°C)	2.7~3.6V	55[1]/70[2]/85ns	10µA	25mA	32-SOP-525, 32-TSOP1-0813.4F 32-TSOP2-400F/R
K6X4008T1F-F	Industrial(-40~85°C)			10µA		
K6X4008T1F-Q	Automotive(-40~125°C)		70[2]/85ns	20µA		32-SOP-525, 32-TSOP1-0813.4F 32-TSOP2-400F

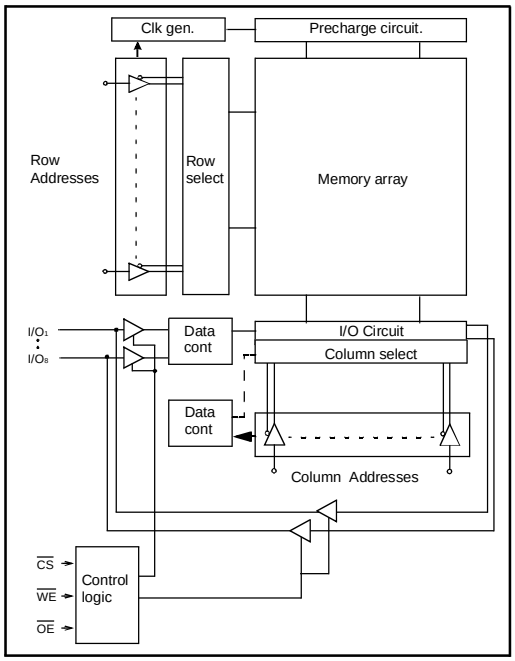
1. This parameter is measured in the voltage range of 3.0V~3.6V with 30pF test load.
2. This parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A_0~A_{18}	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS}$	Chip Select Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input		

FUNCTIONAL BLOCK DIAGRAM



K6X4008T1F Family

PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
K6X4008T1F-GB55[1)] K6X4008T1F-GB70 K6X4008T1F-GB85 K6X4008T1F-YB55[1)] K6X4008T1F-YB70 K6X4008T1F-YB85 K6X4008T1F-VB55[1)] K6X4008T1F-VB70 K6X4008T1F-VB85 K6X4008T1F-MB55[1)] K6X4008T1F-MB70 K6X4008T1F-MB85	32-SOP, 55ns, LL 32-SOP, 70ns, LL 32-SOP, 85ns, LL 32-sTSOP1-F, 55ns, LL 32-sTSOP1-F, 70ns, LL 32-sTSOP1-F, 85ns, LL 32-TSOP2-F, 55ns, LL 32-TSOP2-F, 70ns, LL 32-TSOP2-F, 85ns, LL 32-TSOP2-R, 55ns, LL 32-TSOP2-R, 70ns, LL 32-TSOP2-R, 85ns, LL	K6X4008T1F-GF55[1)] K6X4008T1F-GF70 K6X4008T1F-GF85 K6X4008T1F-YF55[1)] K6X4008T1F-YF70 K6X4008T1F-YF85 K6X4008T1F-VF55[1)] K6X4008T1F-VF70 K6X4008T1F-VF85 K6X4008T1F-MF55[1)] K6X4008T1F-MF70 K6X4008T1F-MF85	32-SOP, 55ns, LL 32-SOP, 70ns, LL 32-SOP, 85ns, LL 32-sTSOP1-F, 55ns, LL 32-sTSOP1-F, 70ns, LL 32-sTSOP1-F, 85ns, LL 32-TSOP2-F, 55ns, LL 32-TSOP2-F, 70ns, LL 32-TSOP2-F, 85ns, LL 32-TSOP2-R, 55ns, LL 32-TSOP2-R, 70ns, LL 32-TSOP2-R, 85ns, LL	K6X4008T1F-GQ70 K6X4008T1F-GQ85 K6X4008T1F-YQ70 K6X4008T1F-YQ85 K6X4008T1F-VQ70 K6X4008T1F-VQ85	32-SOP, 70ns, L 32-SOP, 85ns, L 32-sTSOP1-F, 70ns, L 32-sTSOP1-F, 85ns, L 32-TSOP2-F, 70ns, L 32-TSOP2-F, 85ns, L

1. Operating voltage range is 3.0V~3.6V

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X[1)]	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3(max. 3.9V)	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.9	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	K6F4008T1F-B
		-40 to 85	°C	K6F4008T1F-F
		-40 to 125	°C	K6F4008T1F-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

K6X4008T1F Family

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0/3.3	3.6	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

Note:
1. Commercial Product: T_A=0 to 70°C, otherwise specified
   Industrial Product: T_A=-40 to 85°C, otherwise specified
   Automotive Product: T_A=-40 to 125°C, otherwise specified
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤ 30ns
3. Undershoot: -2.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

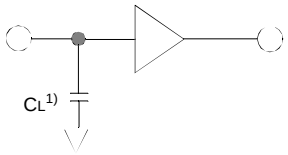
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	2	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA $\overline{CS}$≤0.2V,V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V		-	-	3	mA
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	25	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs = V_{IL} or V_{IH}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc	K6X4008T1F-B	-	-	10	µA
			K6X4008T1F-F	-	-	10	µA
			K6X4008T1F-Q	-	-	20	µA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(see right): C_L=100pF+1TTL
C_L[1)]=30pF+1TTL

1. 55ns, 70ns product



1. Including scope and jig capacitance

AC CHARACTERISTICS

(V_{CC}=2.7~3.6V, Commercial product: T_A=0 to 70°C, Industrial product: T_A=-40 to 85°C, Automotive product: T_A=-40 to 125°C)

Parameter List		Symbol	Speed Bins						Units
			55ns[1)]		70ns		85ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	55	-	70	-	85	-	ns
	Address access time	t_{AA}	-	55	-	70	-	85	ns
	Chip select to output	t_{CO}	-	55	-	70	-	85	ns
	Output enable to valid output	t_{OE}	-	25	-	35	-	40	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	20	0	25	0	25	ns
	Output disable to high-Z output	t_{OHZ}	0	20	0	25	0	25	ns
	Output hold from address change	t_{OH}	10	-	10	-	10	-	ns
Write	Write cycle time	t_{WC}	55	-	70	-	85	-	ns
	Chip select to end of write	t_{CW}	45	-	60	-	70	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	45	-	60	-	70	-	ns
	Write pulse width	t_{WP}	40	-	55	-	55	-	ns
	Write recovery time	t_{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	25	0	25	ns
	Data to write time overlap	t_{DW}	25	-	30	-	35	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	5	-	ns

1. Voltage range is 3.0V~3.6V for commercial and industrial product.

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition		Min	Typ[1)]	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V		2.0	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	K6X4008T1F-B	-	0.5	10	µA
			K6X4008T1F-F	-		10	µA
			K6X4008T1F-Q	-		20	µA
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

1. Typical values are measured at T_A = 25°C and not 100% tested.

MST6151DA-LF

FEATURES

- Input supports up to UXGA & 1080P
- Panel supports up to SXGA
- Integrated two-port triple-ADC/PLL
- Integrated DVI/HDCP/HDMI compliant receiver
- YUV422 digital video input ports
- Dual high-quality scaling engines
- Built-in 3-D video de-interlacer
- Video-over-graphic PIP
- Video-by-graphic split screen
- MStarACE-2 advanced picture/color processing engine
- Embedded On-screen Display Controller (OSD) engine
- Built-in dual-link LVDS transmitter
- 5-Volt tolerant inputs
- Low EMI and power saving features
- Supports PWM & GPO controls
- 208-pin PQFP package

■ Analog RGB/YPbPr Input Ports
- Dual analog ports support up to 165Mhz
- Support PC RGB input up to UXGA@60Hz
- Support HDTV RGB/YPbPr/YCbCr up to 1080P
- On-chip high-performance PLLs
- Support Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

■ DVI/HDCP/HDMI Compliant Input Port
- Operates up to 165 MHz (up to UXGA @60Hz)
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.0 compliant receiver with I2S and S/PDIF digital audio outputs
- Long-cable tolerant robust receiving

■ Video Input Port
- Two 4:2:2 BT656 8-bit digital video input ports
- One 4:2:2 BT601 16-bit digital video input port
- Support 16-bit YUV 4:2:2 interlaced/ progressive video input up to 1080i/720P

■ Auto-Configuration/Auto-Detection
- Auto input signal format (SOG, Composite, Separated HSYNC, VSYNC, and DE), and input mode (all PC & TV modes) detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync Detection for H/V Sync

■ Dual High-Performance Scaling Engines
- Fully Programmable shrink/zoom capabilities
- Nonlinear video scaling supports various modes including Panorama
- Flexible independent control of sharpness for TV and graphic windows

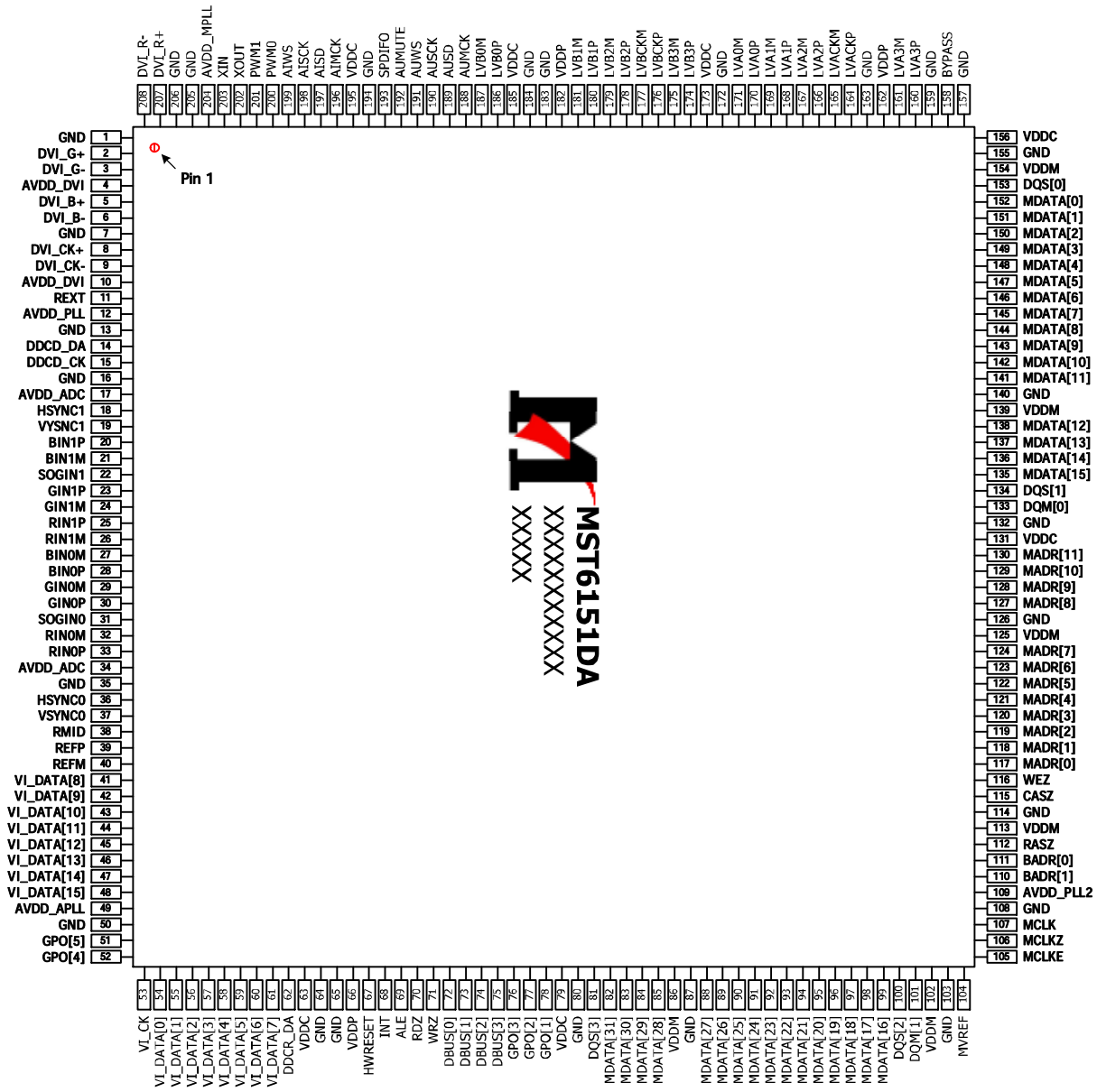
■ Video Processing & Conversion
- 3-D motion adaptive video de-interlacer with edge-oriented adaptive algorithm for smooth low-angle edges
- Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
- PIP with programmable size and location, supports multimedia applications
- Video-over-graphic overlay
- Video-by-graphic split screen
- Frame rate conversion for both main window and sub window
- MStar 2nd Generation Advanced Color Engine (MStarACE-2) automatic picture enhancement gives:
  - Brilliant and fresh color
  - Intensified contrast and details
  - Vivid skin tone
  - Sharp edge
  - Enhanced depth of field perception
  - Accurate and independent color control
- Independent picture control for both main window and sub window
- sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays
- Programmable 10-bit RGB gamma CLUT
- 3-D video noise reduction

- On-Screen OSD Controller
  - 16/256 color palette
  - 256/512 1-bit/pixel font
  - 128/256/512 4-bit/pixel font
  - Supports texture function
  - Supports 4K attribute/code
  - Horizontal and vertical stretch of OSD menus
  - Supports button function
  - Pattern generator for production test
  - Supports OSD MUX and alpha blending capability
  - Supports blinking and scrolling for closed caption applications
- Digital Audio Interface
  - I^2S digital audio input
  - I^2S digital audio output
  - S/PDIF digital audio output
  - HDMI audio channel processing capability
  - Programmable delay for audio/video synchronization
- LVDS Panel Interface
  - Supports dual link up to135MHz dot clock for SXGA
  - Supports 2 data output formats: Thine & TI data mappings
  - Compatible with TIA/EIA
  - With 6/8 bits options
  - Reduced swing for LVDS for low EMI
  - Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation
- External Connection/Component
  - Supports 4-wire double-data-rate direct MCU bus
  - 32-bit data bus for external SDR or DDR SDRAM frame buffer
  - All system clocks synthesized from a single external clock

GENERAL DESCRIPTION

The MST6151DA is a high performance and fully integrated graphics processing IC solution for multi-function LCD monitor/TV with resolutions up to SXGA. It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a video de-interlacer, two high quality scaling engines, an on-screen display controller, and a built-in output clock generator. By use of external frame buffer, PIP is provided for multimedia applications. It supports de-interlaced full-screen video, video-on-graphic overlay, split screen, frame rate conversion, and aspect ratio conversion for various video sources. To further reduce system costs, the MST6151DA also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST6151DA)



PIN DESCRIPTION

MCU Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset, active high	67
DBUS[3:0]	I/O w/ 5V-tolerant	MCU 4-bit DDR Direct bus; 4mA driving strength	75-72
ALE	I w/ 5V-tolerant	MCU Bus ALE, active high	69
RDZ	I w/ 5V-tolerant	MCU Bus RDZ, active high	70
WRZ	I w/ 5V-tolerant	MCU Bus WDZ, active high	71
INT	Output	MCU Bus Interrupt; 4mA driving strength	68

Analog Interface

Pin Name	Pin Type	Function	Pin
RMID		Mid-Scale Voltage Bypass	38
REFP		Internal ADC Top De-coupling Pin	39
REFM		Internal ADC Bottom De-coupling Pin	40
REXT	Analog Input	External Resister 390 ohm to AVDD_DVI	11
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 0	36
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 0	37
BIN0M	Analog Input	Reference Ground for Analog Blue Input from Channel 0	27
BIN0P	Analog Input	Analog Blue Input from Channel 0	28
GIN0M	Analog Input	Reference Ground for Analog Green Input from Channel 0	29
GIN0P	Analog Input	Analog Green Input from Channel 0	30
SOGIN0	Analog Input	Sync On Green Input from Channel 0	31
RIN0M	Analog Input	Reference Ground for Analog Red Input from Channel 0	32
RIN0P	Analog Input	Analog Red Input from Channel 0	33
HSYNC1	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 1	18
VSYNC1	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 1	19
BIN1M	Analog Input	Reference Ground for Analog Blue Input from Channel 1	21
BIN1P	Analog Input	Analog Blue Input from Channel 1	20
SOGIN1	Analog Input	Sync On Green Input from Channel 1	22
GIN1M	Analog Input	Reference Ground for Analog Green Input from Channel 1	24

Pin Name	Pin Type	Function	Pin
GIN1P	Analog Input	Analog Green Input from Channel 1	23
RIN1M	Analog Input	Reference Ground for Analog Red Input from Channel 1	26
RIN1P	Analog Input	Analog Red Input from Channel 1	25

DVI Interface

Pin Name	Pin Type	Function	Pin
DVI_R+	Input	DVI Input Channel Red +	207
DVI_R-	Input	DVI Input Channel Red -	208
DVI_G+	Input	DVI Input Channel Green +	2
DVI_G-	Input	DVI Input Channel Green -	3
DVI_B+	Input	DVI Input Channel Blue +	5
DVI_B-	Input	DVI Input Channel Blue -	6
DVI_CK+	Input	DVI Input Clock +	8
DVI_CK-	Input	DVI Input Clock -	9

Video Interface

Pin Name	Pin Type	Function	Pin
VI_CK	Input w/ 5V-tolerant	Digital Video Input Clock	53
VI_DATA[15:0]	Input w/ 5V-tolerant	Digital Video Input Data[15:0]	48-41, 61-54

Digital Audio Interface

Pin Name	Pin Type	Function	Pin
AUMCK	Output	Audio Master Clock Output	188
AUSD	Output	Audio Serial Data Output; 4mA driving strength	189
AUSCK	Output	Audio Serial Clock Output; 4mA driving strength	190
AUWS	Output	Word Select Output; 4mA driving strength	191
AUMUTE	Output	Audio Output Mute Control	192
SPDIFO	Output	S/PDIF Audio Output; 4mA driving strength	193
AIMCK	Input	Audio Master Clock Input	196
AISD	Input	Audio Serial Data Input	197
AISCK	Input	Audio Serial Clock Input	198
AIWS	Input	Word Select Input	199

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	A-Link Negative LVDS Differential Data Output	171
LVA0P	Output	A-Link Positive LVDS Differential Data Output	170
LVA1M	Output	A-Link Negative LVDS Differential Data Output	169
LVA1P	Output	A-Link Positive LVDS Differential Data Output	168
LVA2M	Output	A-Link Negative LVDS Differential Data Output	167
LVA2P	Output	A-Link Positive LVDS Differential Data Output	166
LVA3M	Output	A-Link Negative LVDS Differential Data Output	161
LVA3P	Output	A-Link Positive LVDS Differential Data Output	160
LVACKM	Output	A-Link Negative LVDS Differential Data Output	165
LVACKP	Output	A-Link Positive LVDS Differential Data Output	164
LVB0M	Output	B-Link Negative LVDS Differential Data Output	187
LVB0P	Output	B-Link Positive LVDS Differential Data Output	186
LVB1M	Output	B-Link Negative LVDS Differential Data Output	181
LVB1P	Output	B-Link Positive LVDS Differential Data Output	180
LVB2M	Output	B-Link Negative LVDS Differential Data Output	179
LVB2P	Output	B-Link Positive LVDS Differential Data Output	178
LVB3M	Output	B-Link Negative LVDS Differential Data Output	175
LVB3P	Output	B-Link Positive LVDS Differential Data Output	174
LVBCKM	Output	B-Link Negative LVDS Differential Data Output	177
LVBCKP	Output	B-Link Positive LVDS Differential Data Output	176

GPO Interface

Pin Name	Pin Type	Function	Pin
PWM0	Output	GPO with PWM Function; 4mA driving strength	200
PWM1	Output	GPO with PWM Function; 4mA driving strength	201
GPO[1]	I/O	GPO / FIELD input; 4mA driving strength	78
GPO[2]	I/O	GPO / Digital VSYNC Input; 4mA driving strength	77
GPO[3]	I/O	GPO / DDC Clock for ROM	76
GPO[4]	I/O	GPO / DE Input; 4mA driving strength	52
GPO[5]	I/O	GPO / Digital HSYNC Input; 4mA driving strength	51

DRAM Interface

Pin Name	Pin Type	Function	Pin
MVREF	Input	Reference Voltage for DDR SDRAM Interface	104
MCLKE	Output	DRAM Memory Clock Enable	105
MCLKZ	Output	DRAM Memory clock Complementary /Input (for differential clocks)	106
MCLK	Output	DRAM Memory Clock	107
RASZ	Output	Row Address Strobe, active low	112
CASZ	Output	Column Address Strobe, active low	115
WEZ	Output	Write Enable, active low	116
DQM[1:0]	Output	Data Mask Byte Enable	101, 133
DQS[3:0]	Output	Data Strobe	81, 100, 134, 153
BADR[1:0]	Output	Memory Bank Address	110, 111
MADR[11:0]	Output	Memory Address	130-127, 124-117
MDATA[31:0]	I/O	Memory Data	82-85, 88-99, 135-138, 141-152

Misc. Interface

Pin Name	Pin Type	Function	Pin
XIN	Crystal Oscillator Input	Crystal Oscillator Input	203
XOUT	Crystal Oscillator Output	Crystal Oscillator Output	202
DDCD_DA	I/O w/ 5V-tolerant	HDCP Serial Bus Data / DDC data of DVI port; 4mA driving strength	14
DDCD_CK	Input w/ 5V-Tolerant	HDCP Serial Bus Clock / DDC Clock of DVI Port	15
DDCR_DA	I/O w/ 5V-tolerant	DDC Data for ROM	62
BYPASS		For External Bypass Capacitor	158

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_DVI	3.3V Power	DVI Power	4, 10
AVDD_ADC	3.3V Power	ADC Power	17, 34
AVDD_PLL	3.3V Power	PLL Power	12
AVDD_PLL2	3.3V Power	PLL Power	109
AVDD_APLL	1.8V Power	Audio PLL Power	49
AVDD_MPLL	3.3V Power	PLL Power	204

S29AL008D

8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

Data Sheet

Distinctive Characteristics

Architectural Advantage

- **Single power supply operation**
  - ? .7 to 3.6 volt read and write operations for battery-powered applications
- **Manufactured on 200nm process technology**
  - ompatible with 0.32 탆 and 230nm Am29LV160 devices
- **Flexible sector architecture**
  - ne 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors (byte mode)
  - ne 8 Kword, two 4 Kword, one 16 Kword, and fifteen 32 Kword sectors (word mode)
  - upports full chip erase
  - ector Protection features:
  - hardware method of locking a sector to prevent any program or erase operations within that sector
  - ectors can be locked in-system or via programming equipment
  - emporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - educes overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - mbedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - mbedded Program algorithm automatically writes and verifies data at specified addresses
- **Compatibility with JEDEC standards**
  - inout and software compatible with single-power supply Flash
  - uperior inadvertent write protection

Performance Characteristics

- **High performance**
  - ccess times as fast as 55 ns
  - xtended temperature range (-40캜 to +125캜)
- **Ultra low power consumption (typical values at 5 MHz)**
  - ? 00 nA Automatic Sleep mode current
  - ? 00 nA standby mode current
  - ? mA read current
  - ? 5 mA program/erase current
- **Cycling endurance: 1,000,000 cycles per sector typical**
- **Data retention: 20 years typical**
  - eliable operation for the life of the system

Package option

- **48-ball FBGA**
- **48-pin TSOP**
- **44-pin SO**

Software Features

- **Data# Polling and toggle bits**
  - rovides a software method of detecting program or erase operation completion
- **Erase Suspend/Erase Resume**
  - uspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation

Hardware Features

- **Ready/Busy# pin (RY/BY#)**
  - rovides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - ardware method to reset the device to reading array data

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Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

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Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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General Description

The S29AL008D is an 8 Mbit, 3.0 volt-only Flash memory organized as 1,048,576 bytes or 524,288 words. The device is offered in 48-ball FBGA, 44-pin SO, and 48-pin TSOP packages. For more information, refer to publication number 21536. The word-wide data (x16) appears on DQ15뻗 Q0; the byte-wide (x8) data appears on DQ7뻗 Q0. This device requires only a single, 3.0 volt V_{CC} supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

This device is manufactured using Spansion뭘200nm process technology, and offers all the features and benefits of the Am29LV800B, which was manufactured using 0.32 탆 process technology.

The standard device offers access times of 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device contains separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm뻚 n internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm뻚 n internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle is completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses are stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

Spansion뭝Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

NTSC ELECTRONIC 2IN1 TUNER

SPECIFICATION

1. APPLICATIONS

1-1. Receiving System : (NTSC M)

1-2. Channel VHF : Low CH. (2) ~ (B)
High CH. (C) ~ (W+11)
UHF : CH. (W+12) ~ (69)

1-3. Intermediate Frequency PIF : (45.75)MHz
CIF : (42.17)MHz
SIF : (41.25)MHz

1-4. Input Impedance : UHF/VHF Terminal (75)Ω, Unbalanced
Output Impedance : (75)Ω, Unbalanced

1-5. Band Change-Over System : (PLL Control System)

1-6. Tuning System : (Electronic Tuning System With PLL)

2. RATINGS AND TEST CONDITIONS

Measurement must be executed under the ambient conditions of the room temperature and humidity. (Temp. 25℃ ±2℃, Humidity 65±5% RH)
The following conditions shall be applied for the measurement of electrical characteristics.

2-1. Environment Conditions

-. Storage Temperature : -20°C ~ +70°C
-. Operation Temperature : -5°C ~ +65°C
-. Relative humidity : 95% MAX.

NTSC ELECTRONIC 2IN1 TUNER

SPECIFICATION

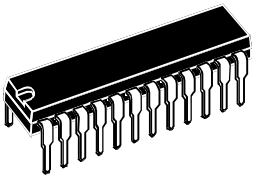
2-2 Voltage Current and Functions At Each Terminal and Operation Guaranteed

PIN NO.	TERMINAL NAME	SUPPLY VOLTAGE FOR OPERATION	GUARANTEED VOLTAGE	CURRENT	FUNCTIONS
1~4	N.C	-	-	-	
5	IF OUT	-	-	-	IF Test Pin
6	N.C	-	-	-	
7	N.C	-	-	-	
8	AGC OUT	-	-	-	AGC VOLT.OUT
9	SAS	-	-	-	IIC Address Select
10	SCL	-	-	-	IIC Serial Clock
11	SDA	-	-	-	IIC Serial Data
12	B+	5V + 0.1V	5V + 5%	170mA MAX (150mA TYP)	Supply Voltage For Tuner Block
13	SIF	-	-	-	Sound IF
14	-	-	-	-	
15	AUDIO OUT	-	-	-	Audio Signal Out
16	AFT OUT	-	-	-	AFT VOLT.OUT
17	VIDEO OUT				Composite Video Baseband Signal Out

TEA6422

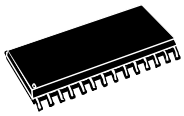
BUS-CONTROLLED AUDIO MATRIX

- 6 Stereo Inputs
- 3 Stereo Ouputs
- Gain Control 0 dB/Mute for each Output
- Cascadable (2 different addresses)
- Serial Bus Controlled
- Very Low Noise
- Very Low Distorsion
- Fully ESD Protected
- Wide Audio Dynamic Range (3 V_{RMS})



SHRINK DIP24
(Shrink Plastic Package)

ORDER CODE: TEA6422



SO28
(Plastic Monopackage)

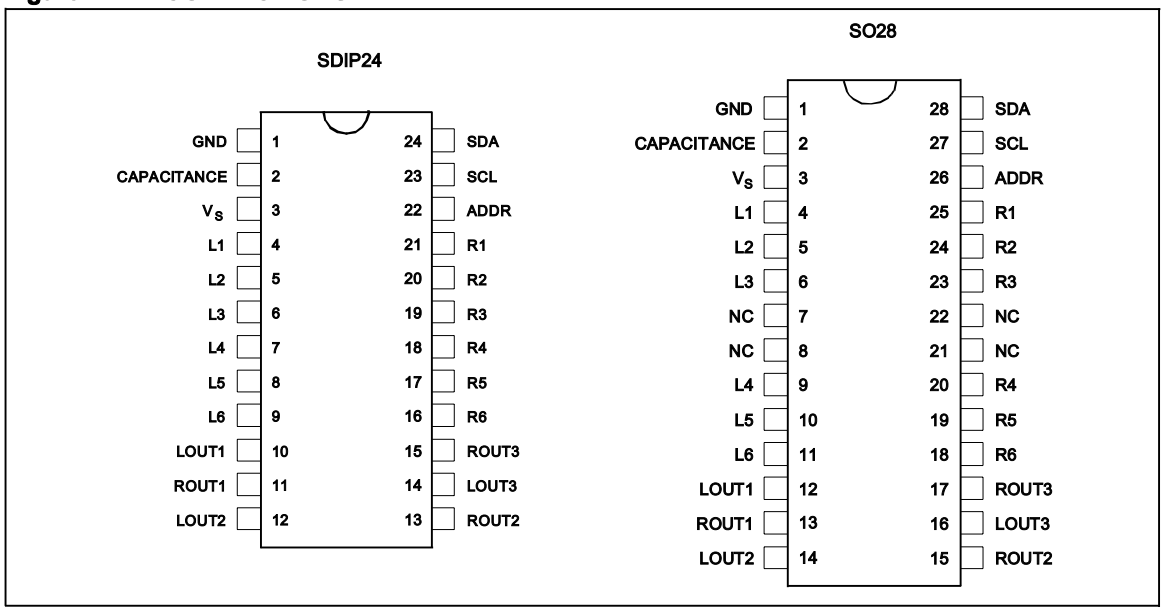
ORDER CODE: TEA6422D

DESCRIPTION

The TEA6422 switches 6 stereo audio inputs on 3 stereo outputs.

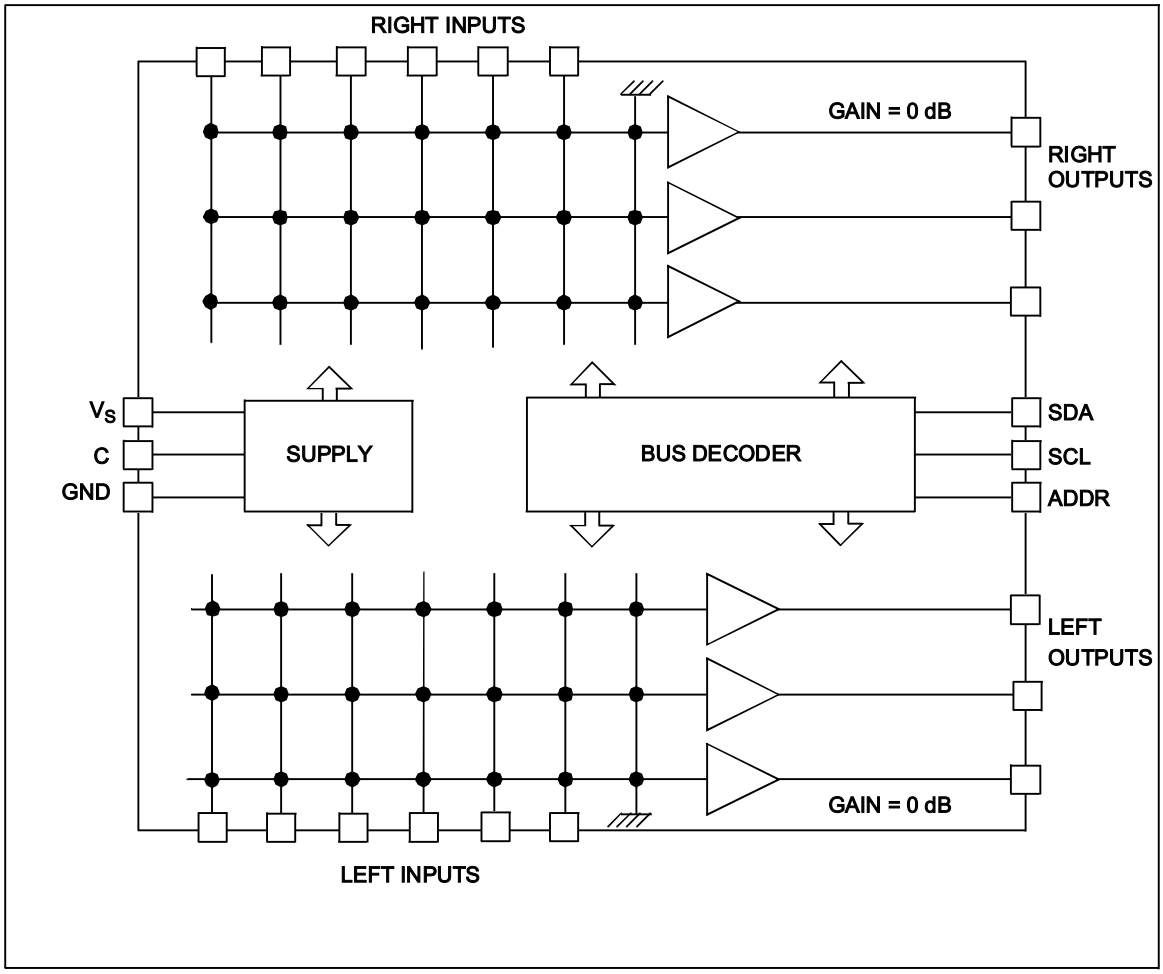
All the switching possibilities are changed through the I^2C BUS.

Figure 1. PIN CONNECTIONS



TEA6422

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12	V
T_{oper}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature	- 20, + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
R_{th}(j-a)	Junction - ambient Thermal Resistance	SDIP24 SO28	75 75	°C/W °C/W

ELECTRICAL CHARACTERISTICS

T_A = 25 °C, V_S = 9 V, R_L = 10 kΩ, R_G = 600 Ω, f = 1 kHz (unless otherwise specified)

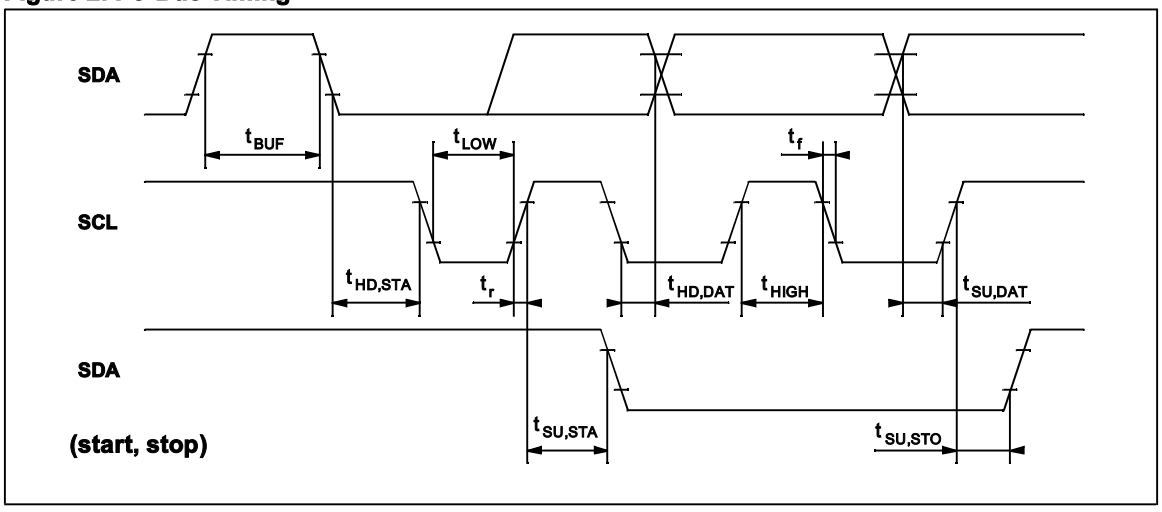
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	10	11	V
I_S	Supply Current			3	8	mA
SVR	Ripple Rejection	V_{IN} = 500mV_{RMS}, f = 1kHz	70	80		dB
MATRIX						
V_{IN}	Input DC Level			V_{CC}/2		V
R_I	Input Resistance		30	50	100	kΩ
C_S	Channel Separation	V_{IN} = 2V_{RMS}, f = 1kHz	80	90		dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level			V_{CC}/2		V
R_{OUT}	Output Resistance			50	100	Ω
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		µV
S/N	Signal to Noise Ratio	V_{IN} = V_{OUT} = 1V_{RMS}		110		dB
G	Gain		-1	0	+ 1	dB
d	Distortion	V_{IN} = V_{OUT} = 1V_{RMS}		0.01	0.05	%
V_{CL}	Clipping Level	d = 0.3 %, V_S = 10 V	2.8	3		V_{RMS}
R_L	Output Load Resistance		2			kΩ

TEA6422

I²C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
SCL					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
f_{SCL}	Clock Frequency		0	100	kHz
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	3V to 1.5V		300	ns
C_I	Input Capacitance			10	pF
SDA					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
C_I	Input Capacitance			10	pF
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	3V to 1.5V		300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA		0.4	V
t_F	Output Fall Time	3V to 1.5V		250	ns
C_L	Load Capacitance			400	pF
TIMING					
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{SU}, DAT	Data Set-up Time		250		ns
t_{HD}, DAT	Data Hold Time		0	340	ns
t_{SU}, STO	Set-up Time from Clock High to Stop		4.0		µs
t_{BUF}	Start Set-up Time following a Stop		4.7		µs
t_{HD}, STA	Start Hold Time		4.0		µs
t_{SU}, STA	Start Set-up Time following Clock Low-to High Transition		4.7		µs

Figure 2. I²C Bus Timing



POWER ON RESET

After power-on reset all outputs are in mute mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}			2.5	V
		Decr. V_{CC}			4.2	V
	End of Reset	Incr. V_{CC}	4.5			V

SOFTWARE SPECIFICATION

1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

Output select

X	0 0 1	0 1 0	X	X	I_2	I_1	I_0	Output 1 Output 2 Output 3

Input select

X	Q_1	Q0	X	X	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 0	Input 1 Input 2 Input 3 Input 4 Input 5 Input 6 Mute

X = don't care - MSB is transmitted first

Example : 010XX100 connects output 3 with input 5.

TEA6422

Figure 3. Distorsion Level versus Input Voltage

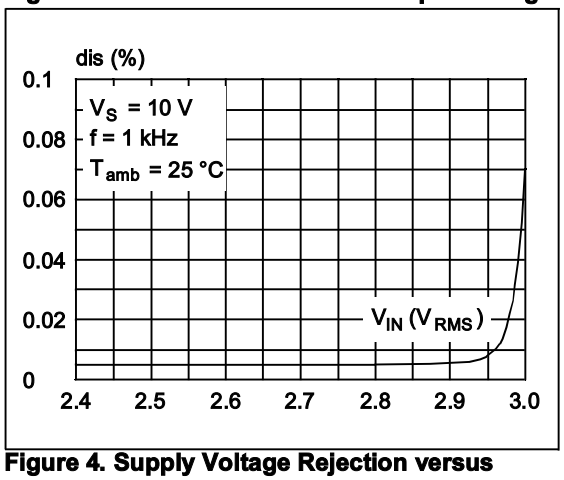


Figure 4. Supply Voltage Rejection versus Frequency (V_{IN} = 500 mV_{RMS})

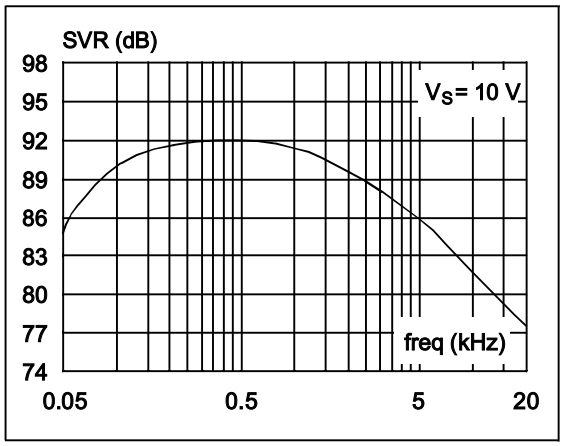
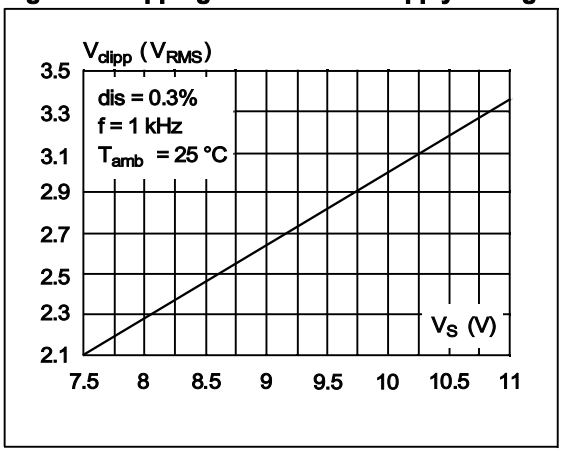


Figure 5. Clipping Level versus Supply Voltage



VI TELEFILTER Filter Specification TFS 36 F 1/5

Description
IF filter for digital cable TV

Measurement condition
Ambient temperature T_A: 25 °C
Input power level: 0 dBm
Terminating impedance: source: 50 Ω
load: 2 kΩ II 3 pF

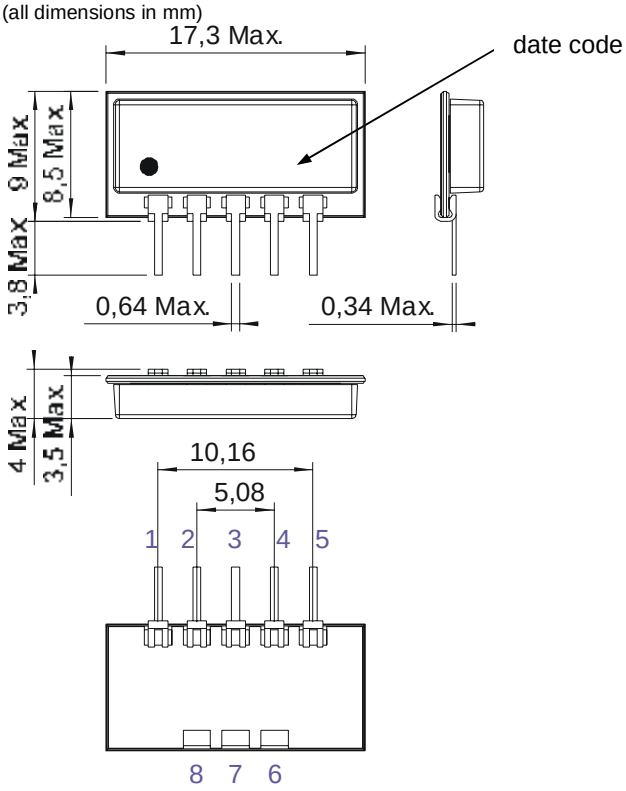
Characteristics
Remark:
Reference level for the relative attenuation a_{rel} of the TFS 36F is the insertion loss. The insertion loss a_e is defined as the insertion loss at the nominal frequency f_N .

D a t a			typ. Value		Limit			
Insertion loss (reference level)			19,6	MHz	20,3	?	1,5	dB
Nominal frequency	f_N		-				36,125	MHz
Centre frequency	f_C at ambient temperature T_A		-		36,125 MHz	?	,055	MHz
Bandwidth	1 dB		7,5	MHz			-	
	3 dB		7,9	MHz			-	
	30 dB		9,3	MHz			-	
Group delay ripple	**p-p in** f_C ? 3,75 MHz		40	ns			-	
Relative attenuation	a_{rel}							
	32,32	MHz	1,6	dB			-	
	39,93	MHz	1,2	dB	1,1	?	1	dB
	32,13	MHz	3,8	dB	3,1	?	1,2	dB
	40,13	MHz	3,4	dB	3,2	?	1,2	dB
	31,25	MHz	41	dB	min.		35	dB
	47,25	MHz	47	dB	min.		42	dB
lower side lobe	25,00 ...29,50	MHz	42	dB	min.		36	dB
	29,50 ...31,25	MHz	39	dB	min.		32	dB
upper side lobe	40,90 ...43,50	MHz	35	dB	min.		32	dB
	43,50 ...50,00	MHz	41	dB	min.		36	dB
Reflected wave signal suppression 1,2 µs ...6,0 µs after main pulse			55	dB	min.		42	dB
Feedthrough signal suppression			53	dB	min.		50	dB
Operable temperature range			-		-25 ...		65	°C
Storage temperature range			-		-40 ...		85	°C
Temperature coefficient of frequency TC_f*			- 0,072	ppm / K			-	

*) ∆

Construction and pin connection

(all dimensions in mm)



1	input
2	input - ground
3	chip carrier - ground
4	output
5	output
6,7,8	internally connected to pin 3

date code:	year + week
N	2001
P	2002
R	2003
...	

Stability Characteristics

After the following tests the filter shall meet the whole specification:

1. Shock:	500g, 18 ms, half sine wave, 3 shocks each plane; DIN IEC 68 T2 - 27
2. Vibration:	10 Hz to 500 Hz, 0,35 mm or 5g respectively, 1 octave per min, 10 cycles per plan, 3 plans; DIN IEC 68 T2 - 6
3. Change of temperature:	-55 캯 to 125캯 / 30 min. each / 10 cycles DIN IEC 68 part 2 ? 14 Test N
4. Resistance to solder heat (reflow):	reflow possible: twice max.; for temperature conditions, please refer to the attached "Air reflow temperature conditions" on page 4;

Packing

Tape & Reel:	DIN IEC 286 ? 3, with exception of value for N and minimum bending radius; tape type II, embossed carrier tape with top cover tape on the upper side;

Air reflow temperature conditions

1st and 2nd air reflow profile

Name:	pre-heating periods	main-heating periods	peak temperature
Temperature:	150 캜 ? 170 캜	over 200 캜	255 캜 ? 5 캜
Time:	60 sec. ? 90 sec.	20 sec. ? 25 sec.	

Chip-mount air reflow profile

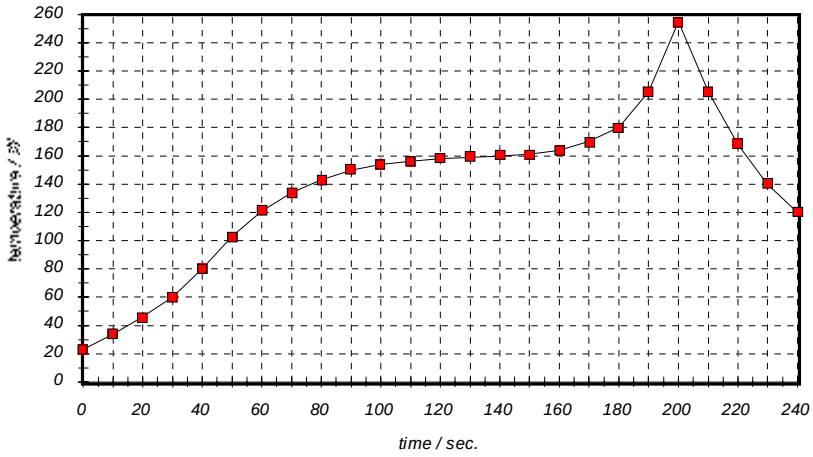


Table for temperature vs. Time during the air reflow process

Tolerance of temperatures: ? 5 캜

time / sec.	Temperature / 캜	time / sec.	Temperature / 캜
0	23	140	160
10	34	150	161
20	46	160	164
30	60	170	170
40	80	180	180
50	103	190	205
60	121	195	230
70	134	200	255
80	143	205	230
90	150	210	205
100	154	215	180
110	156	220	165
120	158	230	140
130	159	240	120

General Description

Release Note: This data sheet describes functions and characteristics of the VCT 49xyl, VCT 48xyl-C4.

1. Introduction

The VCT 49xyl, VCT 48xyl is an IC family of high-quality single-chip TV processors. Modular design and deep-submicron technology allow the economic integration of features in all classes of single-scan TV sets. The VCT 49xyl, VCT 48xyl family is based on functional blocks contained and approved in existing products like DRX 396xA, MSP 34x5G, VSP 94x7B, DDP 3315C, and SDA 55xx.

Each member of the family contains the entire IF, audio, video, display, and deflection processing for 4:3 and 16:9 50/60-Hz mono and stereo TV sets. The integrated microcontroller is supported by a powerful OSD generator with integrated Teletext & CC acquisition including on-chip page memory.

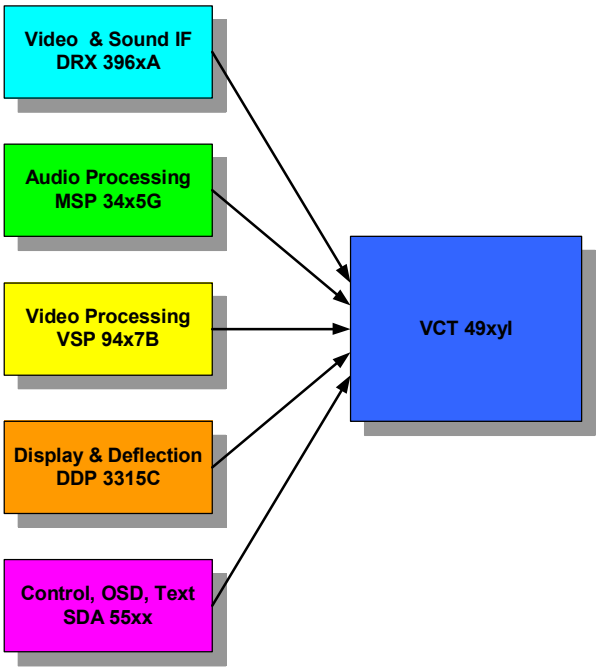


Fig. 1–1: Single-chip VCT 49xyl, VCT 48xyl

1.1. Features

The VCT 49xyl, VCT 48xyl family offers a rich feature set, covering the whole range of state-of-the-art 50/60-Hz TV applications.

- PSSDIP88-1/-2 package
- PMQFP144-2 package
- Submicron CMOS technology
- Low-power standby mode
- Single 20.25 MHz reference crystal
- 8-bit 8051 instruction set compatible CPU
- Up to 256 kB on-chip program ROM
- WST, PDC, VPS, and WSS acquisition
- Closed Caption and V-chip acquisition
- Up to 10 pages on-chip teletext memory
- Multi-standard QSS IF processing with single SAW
- FM Radio and RDS with standard TV tuner
- TV-sound demodulation:
  - all A2 standards
  - all NICAM standards
  - BTSC/SAP with MNR (DBX optional)
  - EIA-J
- Baseband sound processing for loudspeaker channel:
  - volume and balance
  - bass/treble or equalizer
  - loudness and spatial effect (e.g. pseudo stereo)
  - Micronas AROUND (virtual Dolby optional)
  - Micronas BASS
  - further optional and licence requiring sound enhancements as BBE, SRS Wow and Micronas VOICE
- CVBS, S-VHS, YC_rC_b and RGB inputs
- 4H adaptive comb filter (PAL/NTSC)
- multi-standard color decoder (PAL/NTSC/SECAM)
- Nonlinear horizontal scaling “panorama vision”
- Luma and chroma transient improvement (LTI, CTI)
- Non-linear color space enhancement (NCE)
- Dynamic black level expander (BLE)
- Scan velocity modulation output
- Soft start/stop of H-drive
- Vertical angle and bow correction
- Average and peak beam current limiter
- Nonlinear and dynamic EHT compensation
- Black switch off procedure (BSO)

Typical TV Application:	Eco								Basic													Basic 16/9															Advanced		Emu
Features in VCT49xy Versions:	4x21	4x22	4923	4924	4931	4932	4933	4934	4x41	4x42	4943	4944	4x46	4947	4948	4951	4952	4953	4954	4956	4957	4958	4x61	4x62	4963	4964	4x66	4967	4968	4971	4972	4973	4974	4976	4977	4978	4980	4990	49xy
analog sound IF output																																					y	y	y
global analog stereo decoder (A2, EIA-J, BTSC, FM Radio) + auto. stand. detect., STATUS-reg., auto. sound sel., fm-hdev		y	y			y	y			y	y		y	y			y	y		y	y			y	y		y	y			y	y		y	y			y
Radio Data System (RDS)		y	y			y	y			y	y		y	y			y	y		y	y			y	y		y	y			y	y		y	y	y	y	y
NICAM stereo decoder			y				y				y			y				y			y				y			y				y				y			y
stereo baseband processing (bass, treble, loudness, balance, spatial effects) + beeper		y	y	y		y	y	y		y	y	y	y	y	y		y	y	y	y	y	y		y	y	y	y	y	y		y	y	y	y	y	y			y
Micronas BASS, Micronas AROUND virtual, equalizer										y	y	y	y	y	y		y	y	y	y	y	y		y	y	y	y	y	y		y	y	y	y	y	y			y
virtual dolby surround (VDS)													y	y	y					y	y	y					y	y	y					y	y	y			y
4H adaptive comb filter									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
panorama scaler																							y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
2nd RGB/YCrCb input									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
softmix 2nd RGB via fastblank																																					y	y	y
CTI, LTI, histogram									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
dynamic EHT compensation									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
scan velocity modulation (SVM)									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
dynamic focus control																							y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
teletext, VPS, PDC, WSS					y	y	y	y								y	y	y	y	y	y	y								y	y	y	y	y	y	y		y	y
on-chip program ROM	128	128	128	128	128	128	128	128	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256

Common Features:	
IF:	global alignment-free quasi split sound video and sound IF with single SAW
Audio Processing:	global mono audio, mono FM radio, AVC, volume, 2/3 line in, 2/1 line out, 1 speaker out
Color Decoder:	49xy: 11 CVBS/YC/RGB/YCrCb in, 3 CVBS out, global color decoder, 1H NTSC comb filter, blackline detector; 48xy: 11 CVBS/YC/RGB/YCrCb in, 3 CVBS out, NTSC only color decoder, 1H NTSC comb filter, blackline detector
Video Processing:	contrast, saturation, tint, peaking, brightness, gamma, black and blue stretch, programmable RGB matrix
Display Processing:	analog RGB inputs, cutoff and white balance control, beamcurrent limiter
Deflection:	H, V and E/W deflection, H and V EHT compensation, soft start/stop, black switch off, angle and bow, protection circuit
Controller:	CC, V-Chip, ROM, RAM, OSD, DAC, ADC, RTC, timer, watchdog, interrupt controller, UART, I2C bus, Flash version, patch modul
Miscellaneous:	one crystal, few external components, alignment-free

1.2. Chip Architecture

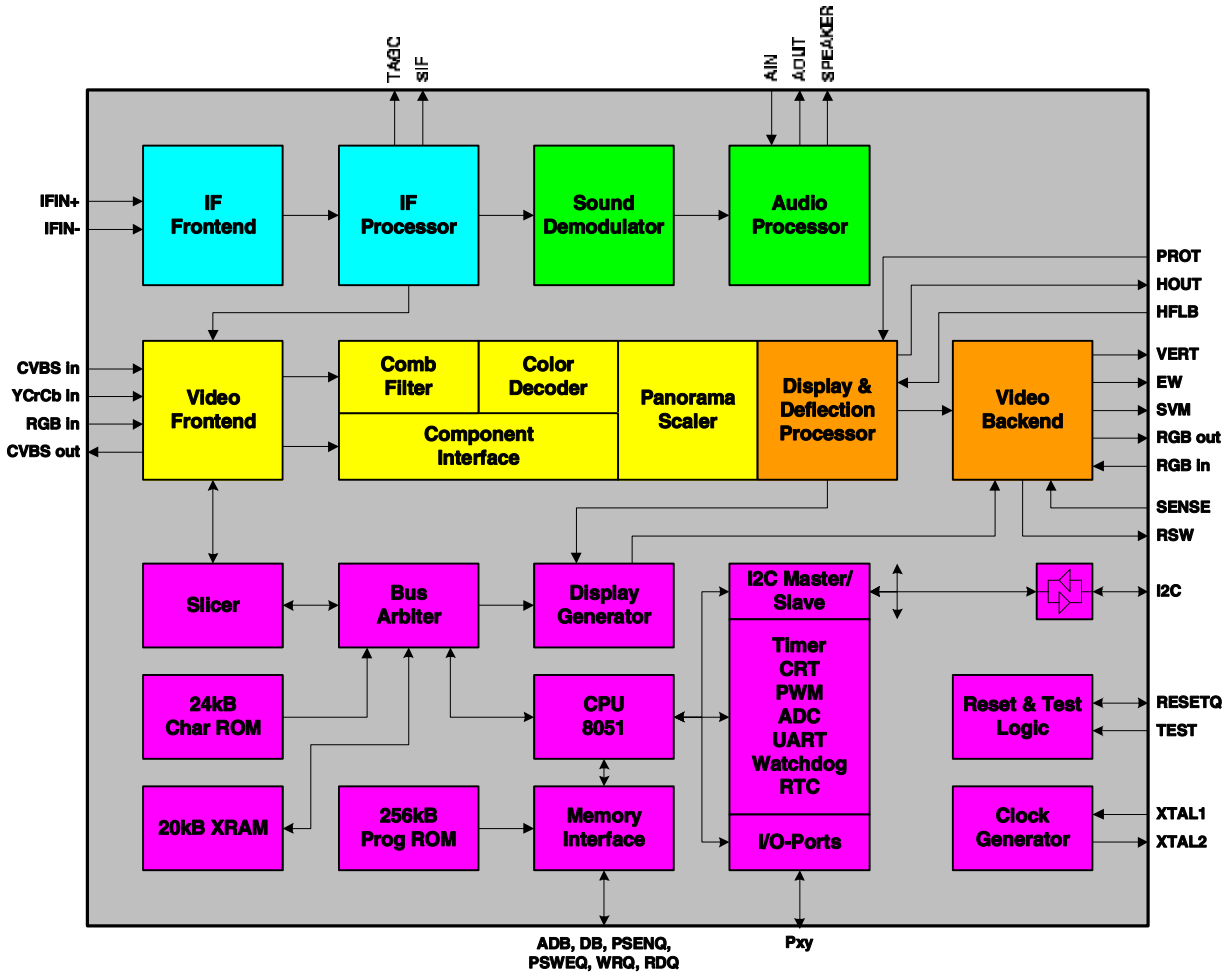


Fig. 1–2: Block diagram of the VCT 49xyl, VCT 48xyl

1.3. System Application

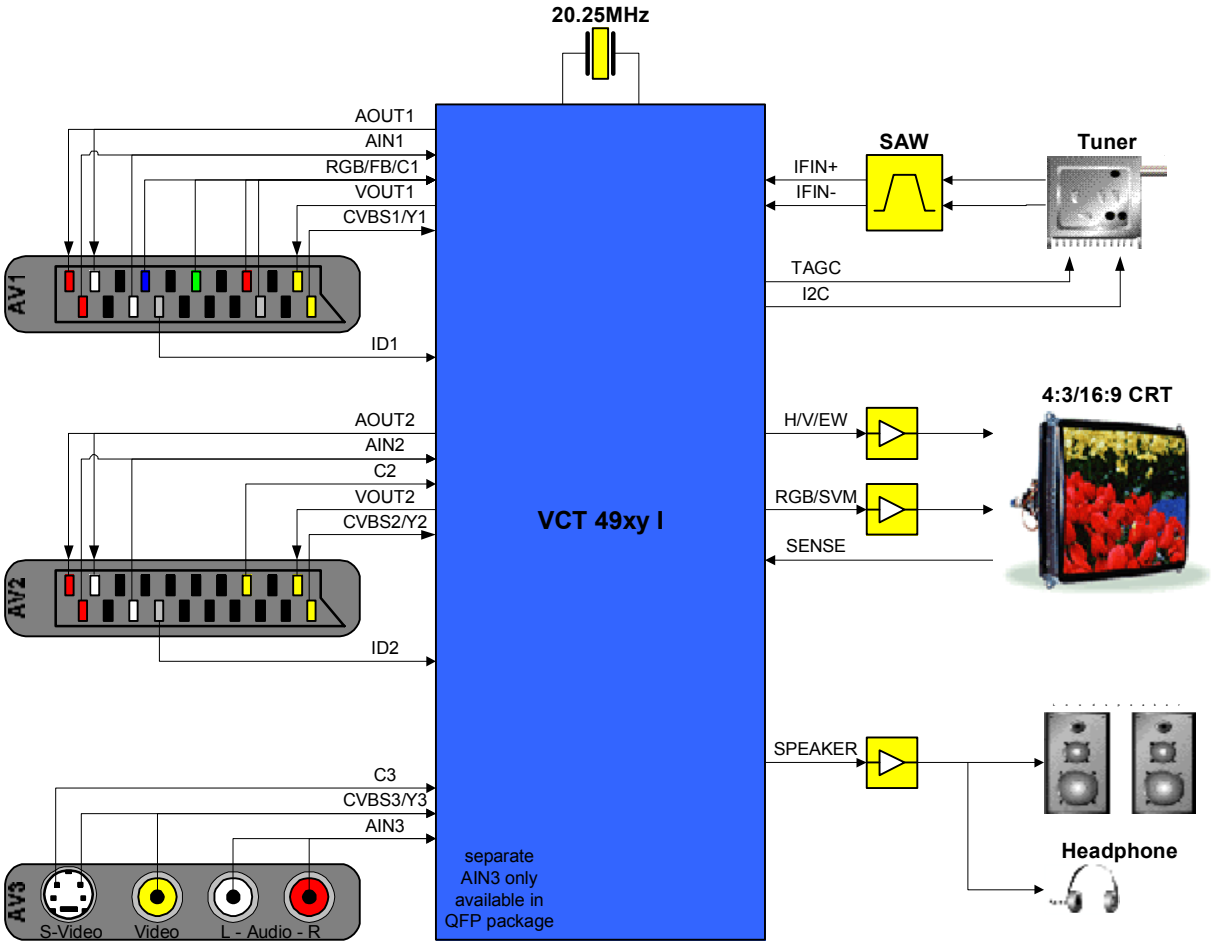


Fig. 1–3: Stereo TV set with VCT 49xyl, VCT 48xyl

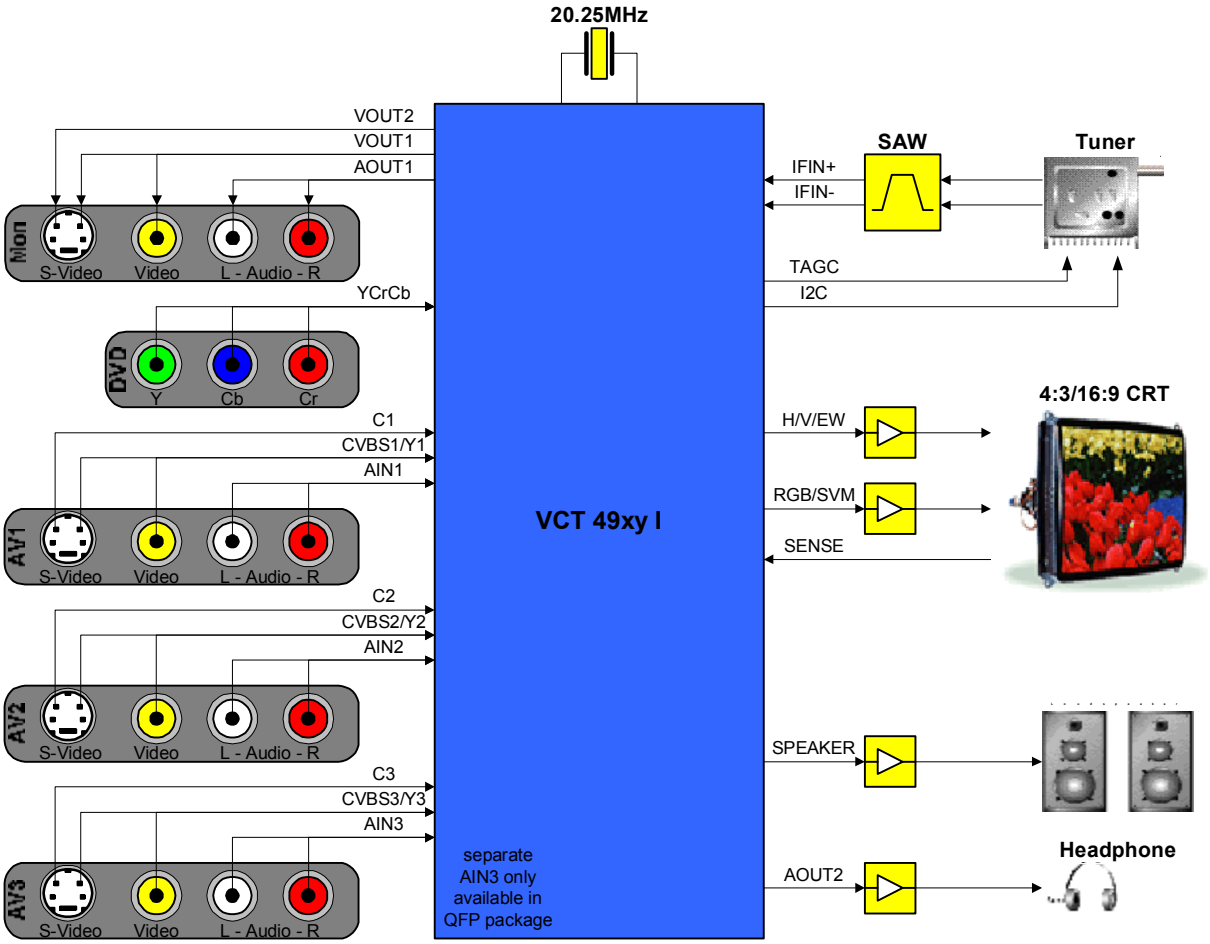


Fig. 1–4: Stereo TV set with VCT 49xyI, VCT 48xyI

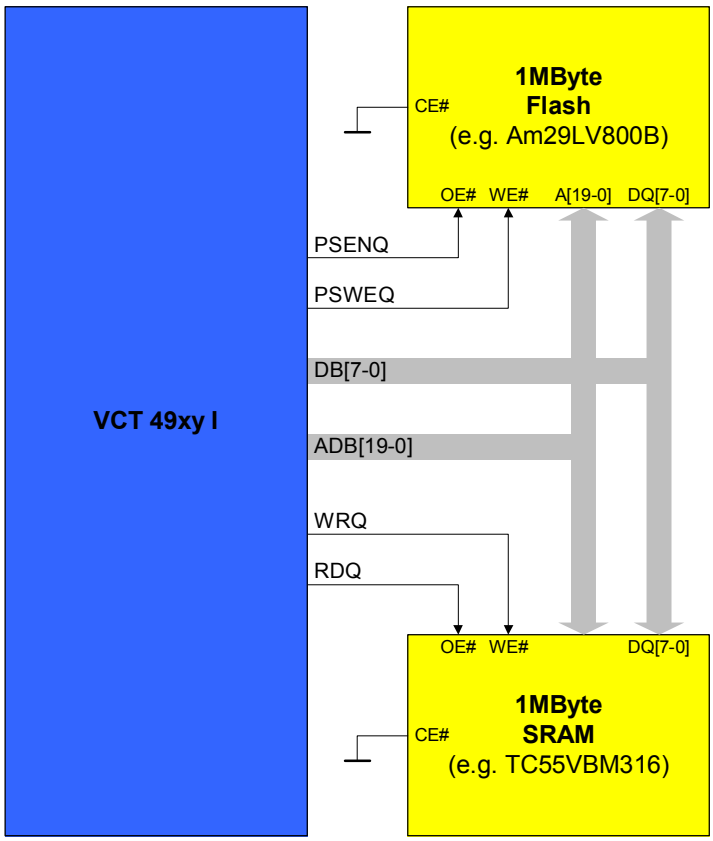


Fig. 1–5: VCT 49xyI, VCT 48xyI application with external program and teletext memory

2. Functional Description

The functional description of the VCT 49xyl, VCT 48xyl is split up into several volumes:

2.1. VCTI

Volume 1: General Description (this document)

2.2. DRX

Volume 2: Digital Receiver Frontend

2.3. MSP

Volume 3: Multistandard Sound Processor

2.4. VSP

Volume 4: Video Processor

2.5. DDP

Volume 5: Display and Deflection Processor

2.6. TVT

Volume 6: Controller, OSD and Text Processing

3. Control Interface

Table 3–1: I2C Slave Device Addresses

Block	8-bit Device Address	
	Write	**Read**
DRX	h'8E	h'8F
MSP	h'8C	h'8D
VSP	h'B0	h'B1
DDP	h'BC	h'BD
TVT	h'D0	h'D1
	programmable via SFR	

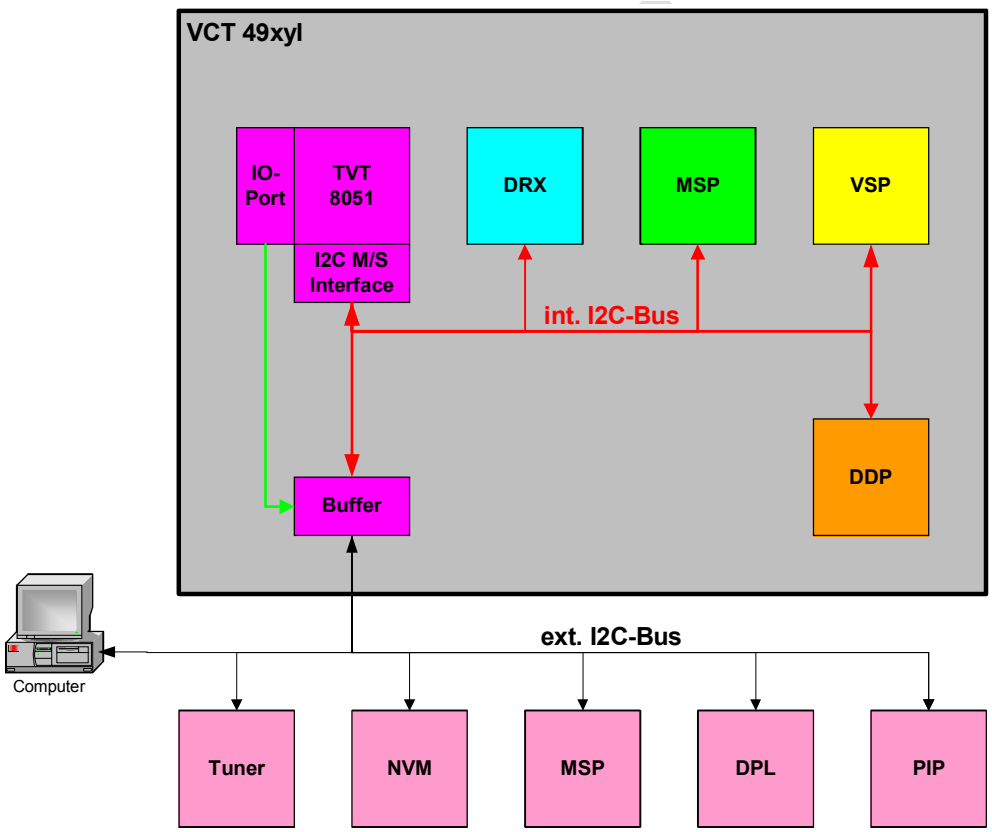
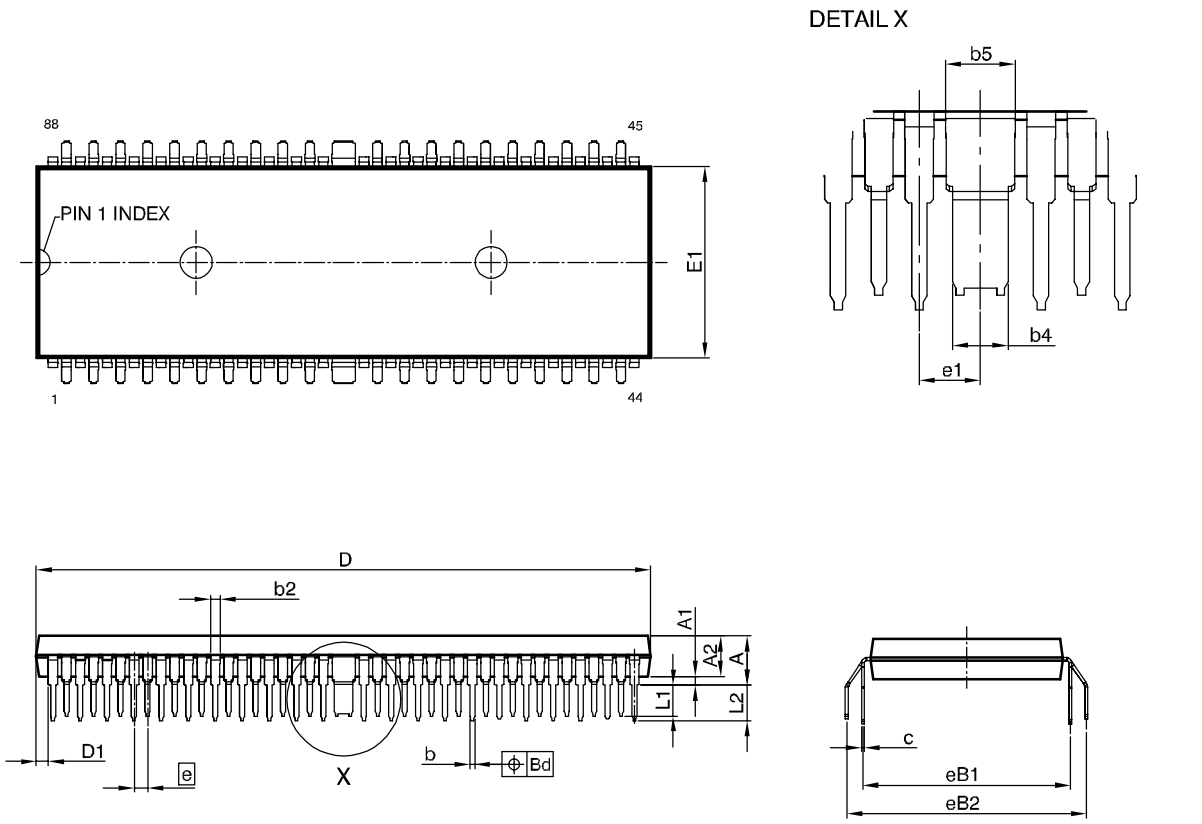


Fig. 3–1: I^2C Environment

4. Specifications

4.1. Outline Dimensions



UNIT	eB2	L1 min	L2 min
mm	22.8 22.2	2.8	3.2

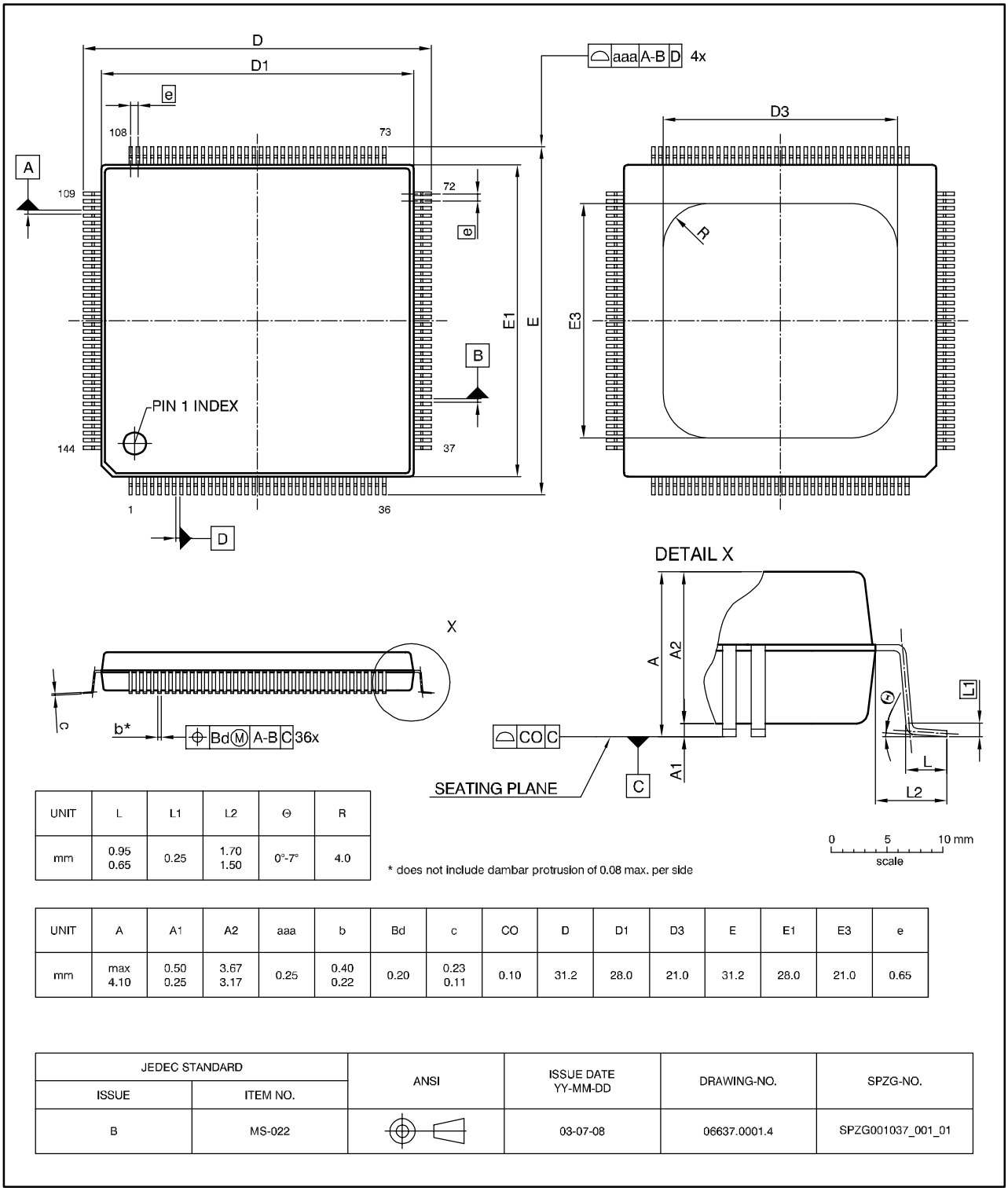
PY Package: Pin 1 Index molded
PZ Package: Pin 1 Index lasered

0 10 20 mm
scale

UNIT	A max	A1 min	A2 max	b	b2	b4	b5	Bd	c	D	D1	E1	e	e1	eB1
mm	4.9	0.5	3.9	0.6 0.4	0.95 0.80	1.85 1.65	2.3 2.1	0.25	0.35 0.20	57.8 57.6	1.21 1.01	18.1 17.9	1.27	1.91	19.8 19.2

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
A	MS-021		03-06-16	06633.0001.4	SPZG001033_001_01

Fig. 4–1:
PSSDIP88-1: Plastic **S**taggered **S**hrink **D**ual **I**n-line **P**ackage, **88** leads, 750 mil
Ordering code: PY or PZ
Weight approximately 9.46 g



UNIT	L	L1	L2	Θ	R
mm	0.95 0.65	0.25	1.70 1.50	0°-7°	4.0

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	D3	E	E1	E3	e
mm	max 4.10	0.50 0.25	3.67 3.17	0.25	0.40 0.22	0.20	0.23 0.11	0.10	31.2	28.0	21.0	31.2	28.0	21.0	0.65

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-07-08	06637.0001.4	SPZG001037_001_01

Fig. 4–2:
PMQFP144-2: Plastic Metric Quad Flat Package, 144 leads, 28 × 28 × 3.4 mm³, 21 × 21 mm² heat slug
Ordering code: XM
Weight approximately 10.1 g

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
IN = Input Pin
OUT = Output Pin
SUPPLY = Supply Pin

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
1	88	128	GND	SUPPLY	OBL	Ground Platform
2	87	129	VSUP5.0BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 5.0 V
3	86	130	TEST	IN	GND	Test Input, reserved for Test
4	85	131	VERT+	OUT	GND	Differential Vertical Sawtooth Output
5	84	132	VERT-	OUT	GND	Differential Vertical Sawtooth Output
6	83	133	EW	OUT	GND	Vertical Parabola Output
7	82	134	RSW2	OUT	LV	Range Switch 2 Output
8	81	135	RSW1	OUT	LV	Range Switch 1 Output
9	80	136	SENSE	IN	GND	Sense ADC Input
10	79	137	GNDM	IN	GND	Reference Ground for Sense ADC
11	78	138	FBIN	IN	GND	Fast Blank Input, Back-end
12	77	139	RIN	IN	GND	Analog Red Input, Back-end
13	76	140	GIN	IN	GND	Analog Green Input, Back-end
14	75	141	BIN	IN	GND	Analog Blue Input, Back-end
15	74	142	SVMOUT	OUT	VSUP5.0BE	Scan Velocity Modulation Output
16	73	143	ROUT	OUT	VSUP5.0BE	Analog Red Output
17	72	144	GOUT	OUT	VSUP5.0BE	Analog Green Output
18	71	1	BOUT	OUT	VSUP5.0BE	Analog Blue Output
19	70	2	VRD		OBL	Reference Voltage for RGB DACs
20	69	3	XREF		OBL	Reference Current for RGB DACs
21	68	4	VSUP3.3BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 3.3 V
22	67	5	GND	SUPPLY	OBL	Ground Platform
23	66	6	GND	SUPPLY	OBL	Ground Platform
24	65	7	VSUP3.3IO	SUPPLY	OBL	Supply Voltage I/O Ports, 3.3 V (main and standby supply)
25	64	8	VSUP3.3DAC	SUPPLY	OBL	Supply Voltage Video DACs, 3.3 V
26	63	9	GNDDAC	SUPPLY	OBL	Ground Video DACs

Volume 1: General Description

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
27	62	10	SAFETY	IN	GND	Safety Input
28	61	11	HFLB	IN	HOUT	Horizontal Flyback Input
29	60	12	HOUT	OUT	LV	Horizontal Drive Output
30	59	13	VPROT	IN	GND	Vertical Protection Input
		37	PWMV	OUT	LV	PWM Vertical Output
		38	DFVBL	OUT	LV	Dynamic Focus Vertical Blanking Output
31	58	39	SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
32	57	40	SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
33	56	41	P21	IN/OUT	LV	Port 2, Bit 1 Input/Output
34	55	42	P20	IN/OUT	LV	Port 2, Bit 0 Input/Output
35	54	43	P17	IN/OUT	LV	Port 1, Bit 7 Input/Output
36	53	44	P16	IN/OUT	LV	Port 1, Bit 6 Input/Output
37	52	45	P15	IN/OUT	LV	Port 1, Bit 5 Input/Output
38	51	46	P14	IN/OUT	LV	Port 1, Bit 4 Input/Output
39	50	47	P13	IN/OUT	LV	Port 1, Bit 3 Input/Output
40	49	48	P12	IN/OUT	LV	Port 1, Bit 2 Input/Output
41	48	49	P11	IN/OUT	LV	Port 1, Bit 1 Input/Output
42	47	50	P10	IN/OUT	LV	Port 1, Bit 0 Input/Output
43	46	53	VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 3.3 V (main and standby supply)
44	45	54	GND	SUPPLY	OBL	Ground Platform
45	44	55	GND	SUPPLY	OBL	Ground Platform
46	43	56	VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 1.8 V (main and standby supply)
47	42	57	VOUT3	OUT	LV	Analog Video 3 Output
48	41	58	VOUT2	OUT	LV	Analog Video 2 Output
49	40	59	VOUT1	OUT	LV	Analog Video 1 Output
50	39	60	VIN1	IN	GND	Analog Video 1 Input
51	38	61	VIN2	IN	GND	Analog Video 2 Input
52	37	62	VIN3	IN	GND	Analog Video 3 Input
53	36	63	VIN4	IN	GND	Analog Video 4 Input
54	35	64	VIN5	IN	GND	Analog Video 5 Input
55	34	65	VIN6	IN	GND	Analog Video 6 Input
56	33	66	VIN7	IN	GND	Analog Video 7 Input

Volume 1: General Description

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
84	5	123	SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right
85	4	124	SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
86	3	125	VREFAU		OBL	Reference Voltage, Audio
87	2	126	VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
88	1	127	GND	SUPPLY	OBL	Ground Platform
		71	P37 / 656IO7	IN/OUT	LV	Port 3, Bit 7 Input/Output Digital 656 Bus 7 Input/Output
		72	P36 / 656IO6	IN/OUT	LV	Port 3, Bit 6 Input/Output Digital 656 Bus 6 Input/Output
		73	P35 / 656IO5	IN/OUT	LV	Port 3, Bit 5 Input/Output Digital 656 Bus 5 Input/Output
		74	P34 / 656IO4	IN/OUT	LV	Port 3, Bit 4 Input/Output Digital 656 Bus 4 Input/Output
		75	P33 / 656IO3	IN/OUT	LV	Port 3, Bit 3 Input/Output Digital 656 Bus 3 Input/Output
		76	GNDEIO	SUPPLY	OBL	Ground Extended I/O Ports
		77	VSUP3.3EIO	SUPPLY	OBL	Supply Voltage Extended I/O Ports, 3.3 V
		78	P32 / 656IO2	IN/OUT	LV	Port 3, Bit 2 Input/Output Digital 656 Bus 2 Input/Output
		79	P31 / 656IO1	IN/OUT	LV	Port 3, Bit 1 Input/Output Digital 656 Bus 1 Input/Output
		80	P30 / 656IO0	IN/OUT	LV	Port 3, Bit 0 Input/Output Digital 656 Bus 0 Input/Output
		81	P26 / 656VIO	IN/OUT	LV	Port 2, Bit 6 Input/Output Digital 656 Vsync Input/Output
		82	P25 / 656HIO	IN/OUT	LV	Port 2, Bit 5 Input/Output Digital 656 Hsync Input/Output
		83	P24 / 656CLKIO	IN/OUT	LV	Port 2, Bit 4 Input/Output Digital 656 Clock Input/Output
		31	ADB19	OUT	LV	Address Bus 19 Output
		21	ADB18	OUT	LV	Address Bus 18 Output
		19	ADB17	OUT	LV	Address Bus 17 Output
		22	ADB16	OUT	LV	Address Bus 16 Output
		23	ADB15	OUT	LV	Address Bus 15 Output
		18	ADB14	OUT	LV	Address Bus 14 Output
		17	ADB13	OUT	LV	Address Bus 13 Output
		26	ADB12	OUT	LV	Address Bus 12 Output

VCT 49xyl, VCT 48xyl

ADVANCE INFORMATION

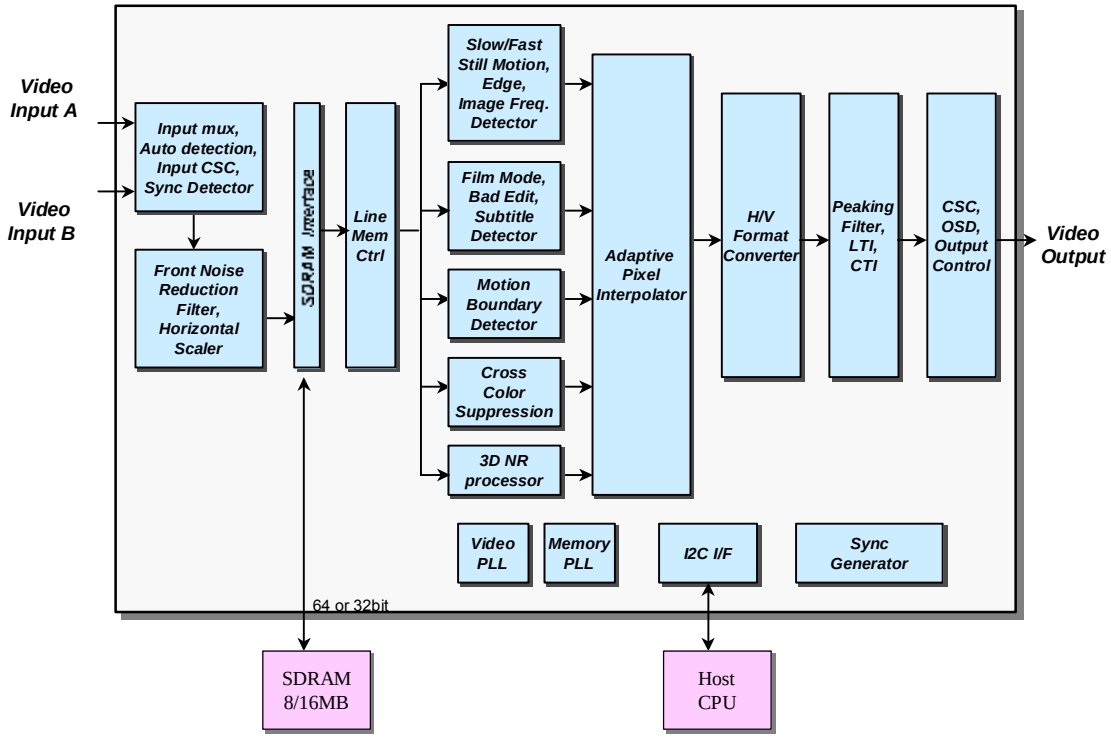
Volume 1: General Description

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
		14	ADB11	OUT	LV	Address Bus 11 Output
		96	ADB10	OUT	LV	Address Bus 10 Output
		15	ADB9	OUT	LV	Address Bus 9 Output
		16	ADB8	OUT	LV	Address Bus 8 Output
		27	ADB7	OUT	LV	Address Bus 7 Output
		28	ADB6	OUT	LV	Address Bus 6 Output
		29	ADB5	OUT	LV	Address Bus 5 Output
		30	ADB4	OUT	LV	Address Bus 4 Output
		84	ADB3	OUT	LV	Address Bus 3 Output
		85	ADB2	OUT	LV	Address Bus 2 Output
		86	ADB1	OUT	LV	Address Bus 1 Output
		87	ADB0	OUT	LV	Address Bus 0 Output
		88	DB0	IN/OUT	LV	Data Bus 0 Input/Output
		89	DB1	IN/OUT	LV	Data Bus 1 Input/Output
		90	DB2	IN/OUT	LV	Data Bus 2 Input/Output
		91	DB3	IN/OUT	LV	Data Bus 3 Input/Output
		92	DB4	IN/OUT	LV	Data Bus 4 Input/Output
		93	DB5	IN/OUT	LV	Data Bus 5 Input/Output
		94	DB6	IN/OUT	LV	Data Bus 6 Input/Output
		95	DB7	IN/OUT	LV	Data Bus 7 Input/Output
		32	RDQ	OUT	LV	$\overline{\text{Data Read Enable}}$ Output
		33	WRQ	OUT	LV	$\overline{\text{Data Write Enable}}$ Output
		34	OCF	OUT	LV	Opcode Fetch Output
		35	ALE	OUT	LV	Address Latch Enable Output
		36	RSTQ	OUT	LV	$\overline{\text{Internal CPU Reset}}$ Output
		97	PSENQ	OUT	LV	$\overline{\text{Program Store Enable}}$ Output
		20	PSWEQ	OUT	LV	$\overline{\text{Program Store Write Enable}}$ Output
		51	XROMQ	IN	OBL	$\overline{\text{External ROM Enable}}$ Input
		52	EXTIFQ	IN	LV	$\overline{\text{Enable External Interface}}$ Input
		24	STOPQ	IN	LV	$\overline{\text{Stop CPU}}$ Input
		25	ENEQ	IN	LV	$\overline{\text{Enable Emulation}}$ Input

MDIN180

MDIN-180 is a highly integrated single chip implementation of deinterlacing and format conversion. MDIN-180 provides configurable digital video input ports for interlaced or progressive scan type video with 10bit precision per color component and one digital output port for progressive scan type of digital video stream with 10bit precision per color component. MDIN-180 receives any format of interlaced scan type video and performs deinterlacing and format conversion to produce any desired format of progressive scan video with excellent signal quality preservation. MDIN-180 provides high quality edge preserving deinterlacing with up-to-date motion adaptation algorithm with fast motion and film mode detection and proper deinterlacing and it supports high performance 3D noise reduction and cross color suppression. In addition MDIN-180 scales up or down the input video with an arbitrary scale ratio and it also provides frame rate conversion capability.
MDIN-180's high quality deinterlacing and video processing capability is suitable for high quality display format conversion application such as flat panel display TV, high-end progressive display, and so on.

Block Diagram



Main Features

- Configurable two digital video input ports for interlaced or progressive 30/24-bit RGB, 30/24-bit YCbCr 4:4:4, 20/16-bit YCbCr 4:2:2, 20/16-bit Y/C separated, 10/8-bit Y/C multiplexed digital format.
- Generates the progressive scanned digital video output up to 1536x1080p
- Performs high quality deinterlacing for arbitrary format of interlaced video input up to 1080i
- Motion adaptive 3-D deinterlacing with pixel-by-pixel motion adaptive interpolation
- High quality edge preserving deinterlacing thru multiple directional edge detection and interpolation
- Deinterlacing with fast motion detection and processing using recent 30 fields motion information
- Deinterlacing with motion boundary preservation using recent 30 fields motion information
- Deinterlacing with film mode detection and processing for film source
- Deinterlacing with bad edit and subtitle detection and adaptation for film source
- 3D noise reduction in both temporal and spatial domain
- Cross color suppression for the video without being processed by 3D comb filter
- Independent horizontal and vertical scaling
- Frame rate conversion with arbitrary conversion ratio
- Programmable front noise reduction filter for input video
- One dimensional LTI and CTI for edge improvement
- Programmable high order peaking filter for horizontal sharpness control
- Color enhancement filter for smooth color component output
- Programmable brightness, contrast, tint and saturation control
- One layer bitmap OSD with 4 sprite and 16 color
- Seamless interface to 8MB or 16MB SDRAM widely available in the market
- Serial I2C interface

Specifications

- Input Formats
  - Configurable two input ports : Total 40-bit configurable. 30-bit + 10bit, 24-bit + 16-bit, 20-bit + 20-bit etc. with 10-bit or 8-bit per color component
  - Video Sources : 30-bit RGB, YcbCr 4:4:4, 20-bit YcbCr 4:2:2, 20-bit Y/C seperated digital format (SMPTE274M etc.), 10-bit Y/C multiplexed digital format(CCIR-656 etc.)
  - Maximum Pixel Rate : 108Mpixel/sec
  - Interlaced Input : standard or non-standard video format up to 1920x1080i 60Hz
  - Progressive Input : standard or non-standard video format up to 1280x1024p 60Hz

- Output Formats
  - Progressive digital RGB, YCbCr 4:4:4 or YcbCr 4:2:2 or 16-bit Y/C separated digital format with 10-bit per color component
  - Programmable output mode : 30-bit single width pixel mode
  - Maximum Pixel Rate : 115Mpixel/sec
  - Programmable display format standard or non-standard video format up to 1536x1080p

- Format Conversion
  - Independent horizontal and vertical scaling
  - Format conversion from one format to another format at an arbitrary scaling ratio
  - Horizontal and vertical anti-aliasing filters for graceful down conversion

- Frame Rate Conversion
  - Frame rate conversion from 3~250Hz to 3~250Hz
  - Conversion ratio : x1/31 to x31
  - Uses external SDRAM as frame buffer

- Deinterlace
  - Deinterlacing for any interlaced input video up to 1080i
  - Motion adaptive 3-D deinterlace using 5 fields on a per-pixel basis
  - Programmable motion detection and adaptation control
  - Adaptive motion-weighted interpolation for eliminating non-motion artifacts
  - Multi-directional edge preserving interpolation
  - Fast motion detect and handling using recent 30 fields motion information
  - Motion boundary preservation using recent 30 fields motion information
  - Still Mode for crisp image viewing
  - 3:2 or 2:2 pull-down film mode detect and handling
  - Bad edit detect and handling
  - Still and moving subtitle detect and handling

- Noise Reduction and Signal Enhancement Filter
  - Programmable front noise reduction filter for input video
  - 3D noise reduction in both temporal and spatial domain
  - One dimensional LTI and CTI for edge enhancement
  - Programmable high order peaking filter for horizontal sharpness control
  - Color enhancement filter for smooth color component output

- Display Functions
  - Programmable sizing & positioning
  - YCbCr-to-RGB color space conversion with programmable 3x3 matrix
  - Programmable brightness, contrast, tint and saturation control
  - One layer bitmap OSD with 4 sprite and 16 color

- Frame Buffer Memory
  - 8MB or 16MB external SDRAM
  - 32-bit or 64-bit data width interface
  - Seamless interface to widely available x16 or x32-bit SDRAM

- Serial Bus Interface & Interrupt
  - I2C bus interface
  - Interrupt signal to an external host processor

- Miscellaneous
  - Auto detection of input video/sync type and format
  - Auto detection of input video/sync changing and lost
  - Sync detection for composite and non-standard input sync
  - Input-frame-locking mode and free-run mode
  - Programmable output sync generation
  - Built-in input/output test pattern generator

- Electrical and Mechanical Characteristics
  - 1.8V and 3.3V supply voltage, 5V tolerant I/O
  - 256-pin BGA package

LC3701E PART LIST

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
1	1	B4204678050	KIT LAB & MAN,E370D DVB-T MZE/SKD(SILVER	
2	1	6316349421	STICKER RoHS ELO ALL	
3	1	6316349466	STICKER,SHIPPING LABEL E370D MARANTZ	
4	1	6316379729	BACK LABEL E370D/E420D MARANTZ	
5	1	6320239072	MANUAL ASS'Y E370D/E420D MARANTZ/DVB-T	
6	1	6243037901	MANUAL PE BAG	
7	1	6320240108	MANUAL U/G, E370D/E420D MARANTZ/DVB-T	
8	1	B4210347700	SCREW ASSY,E370D HIE SKD	
9	12	5001000681	SCR-WSP,MC(+)3*5[S]	
10	4	5001000684	SCR-WSP,MC(+)3*8[S]	
11	4	5001000686	SCR-BIN,MC(+)4*10[B]	
12	4	5001000712	SCR-BIN,MC(+)8*14[B]	
13	6	5001000714	SCR-BIN,MC(+)4*10[S]	
14	4	5001000716	SCR-BIN,(T/SP)MC(+)4*6[S]	
15	4	5001000727	SCR-HEX,UNC #4-40*11.8[S]	
16	8	5001000748	SCR-BIN(SP),MC(+)4*12[S]	
17	6	5001000752	SCR-BIN(SP),MC(+) 4*16[B]	
18	5	5004000197	SCR-BIN,TT2(+)3*10[S]	
19	11	5004000223	SCR-BIN,TT2(+)3*8[B]	
20	30	5004000228	SCR-BIN,TT2(+)4*14[B]	
21	4	5401000087	WASH-PL,8[B]	
22	4	5402000002	WASH-SP,8[B]	
23	1	6128010197	GASKET EMI,12x15Tx30	
24	1	B4210347800	ETC ASSY,E370D HIE SKD	
25	1	6128010215	GASKET EMI,20X21TX45	
26	1	6128010232	FABRIC GASKET,10x9Tx15(FAB)	
27	1	6210107111	AL TAPE, 80X80	
28	2	6210109600	AL TAPE,35x35	
29	1	6210109700	FABRIC TAPE,30x100	
30	3	6223088700	WIRE SADDLE,H=18.2	
31	1	6225033900	INSULATION SHEET,E420	
32	1	E4205029702	MAIN ASSY(M1)/L,E370 DVB-T(W/O PCB'A)	
33	1	3010701072	IR B/D ASSY,E SERIES DVB-T	

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
34	1	361020013202	PWR-SPPLY,26/32" DTV 24V/12V/STB5V/30V	
35	1	3725005522	CONN-A,14P INVERTER CBL/Q320	
36	1	3725005523	CONN-A,15P POWER CABLE/Q320 ATSC	
37	1	3725005561	CONN-A,6P ATV/DTV VIDEO CBL/Q320 DVB-T	
38	1	3725005664	CONN-A,MAIN PWR SWITCH CBL 400MM E MODEL	
39	1	3725005668	CONN-A,LG LVDS CBL E370 DVB-T	
40	1	3725005670	CONN-A,OSD CBL 26/32/37 E-SERIES JPN/DVB	
41	1	3725005672	CONN-A,SPK CBL-L,32/37 E-Series JPN/DVB	
42	1	372500567201	CONN-A,SPK CBL-R 32/37 E-Series JPN/DVB	
43	1	E42077080050	CBL-PWR,BK WALL EUROPE 1.83MT	
44	1	3010701037	REMOTE CONTROL ASSY,DVB-T KRC-61	
45	1	3010701056	KEY B/D ASSY,E-SERIES JPN/DVB-T	
46	1	3550100151	SPEAKER,E370D BOTTOM	
47	1	372500531201	CONN-A,PAL CABLE 3.0M MALE <-> FEMALE	
48	1	6101235480	MAIN FRAME ASSY,E370D DVB-T SKD(10)	
49	1	6101235400	MAIN FRAME ASSY,E370D DVB-T	
50	1	6101234800	MAIN FRAME,E370	
51	4	6128010239	GASKET EMI,20X12TX70(FAB,PLP)	
52	0.1	6301207600	SKD BOX,E370 MAIN FRAME ASSY 530x265x330	
53	2	6110291480	BRKT BEAM,E370 SKD(20)	
54	1	6110291400	BRKT BEAM,E370	
55	0.05	6301207700	SKD BOX,E370 BRKT BEAM 600x460x145(예일)	
56	1	6110291780	PORT BRKT BTM,E370 SKD(60)	
57	1	6110291700	PORT BRKT BOTTOM,E370	
58	0.017	6301207900	SKD BOX,E370 PORT BRKT BTM 530x145x85(화	
59	1	6110291980	SIDE BRKT,E370 SKD(200)	
60	1	6110291900	SIDE BRKT,E420	
61	0.005	6301208000	SKD BOX,E370 SIDE BRKT 350x350x150(휴먼)	
62	1	6110292080	STAND BEAM,E370 SKD(14)	
63	1	6110292000	STAND BEAM,E370	
64	0.072	6301207800	SKD BOX,E370 STAND BEAM 595x235x165(예일	
65	1	6201351581	COVER REAR,E370(NO LOGO) SKD(8)	
66	1	6201351501	COVER REAR,E370(NO LOGO)	
67	0.125	6301207400	SKD BOX,E370 COVER 970x540x620(세화)	
68	1	6201352080	CAP PORT SIDE,E420 SKD(400)	

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
69	1	6201352000	CAP PORT SIDE,E420	
70	0.003	6301207500	SKD BOX,E370 CAP PORT SIDE 500x500x350(	
71	1	6201353481	COVER F,ASSY E370 DVB-T MZE SKD(12)	
72	1	6201353404	COVER F,ASSY E370 DVB-T MZE	
73	1	6201351400	COVER FRONT,E370	
74	1	6201361500	DECO PANEL E370(ACRYL)/MZE	
75	1	6210336400	LOGO PLATE (PDP)	
76	0.083	6301207400	SKD BOX,E370 COVER 970x540x620(세화)	
77	1	6201353681	STAND BASE ASSY,E370 SKD(8)	
78	9	5004000217	SCR-BIN,TT2(+)4*10[S]	
79	1	6101235000	STAND BASE FRAME SQUARE,E420	
80	1	6201352100	STAND BASE SQUARE,E420	
81	4	6261050600	RUBBER FOOT Φ19.0 4.0T	
82	5	6261050700	RUBBER FOOT Φ19.0 4.5T	
83	0.125	6301208200	SKD BOX,E370 BASE ASSY 570x215x320(동산)	
84	1	6201353684	STAND BODY ASSY(BK2,SP) E370D SKD(6)	
85	7	5004000248	SCR-BIN,TT2(+)4*14[S]	
86	7	5004000252	SCR-FLT,TT2(+)4*14[S]	
87	1	6110292600	BODY SQUARE,E420	
88	1	6110292702	BODY BRKT(BK,SP) E420	
89	1	6115029301	SWIVEL ASSY,E420	
90	1	6110292800	SWIVEL TOP BRKT,E420	
91	1	6110292900	SWIVEL BOTTOM BRKT,E420	
92	1	6120342700	SWIVEL DECO,E420	
93	1	6201352201	BODY CAP,E420(BK)	
94	0.17	6301208100	SKD BOX,E370 BODY ASSY 520x340x240(동산)	
95	4	6223088400	42INCH PDP BOX HOLDER	
96	1	6242034500	BOTTOM PORT LABEL,E420 DVB-T	
97	1	6242034600	SIDE PORT LABEL E420 DVB-T	
98	1	6243038306	PE BAG(SET),Q400	
99	1	6253130200	CUSHION TOP "L",E370	
100	1	6253130201	CUSHION TOP "R",E370	
101	1	6253130300	CUSHION BOTTOM "L",E370	
102	1	6253130301	CUSHION BOTTOM "R",E370	
103	1	6301204100	ACCESSORY BOX,Q400	

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
104	1	6301205502	CTN BOX,DW-3 E37*D MARAMTZ	
105	1	6301205600	CTN BOX,DW-3 E370D BOTTOM	
106	1.5	6316349238	LABEL SHIPPING,ELO(W/T)-80*40	

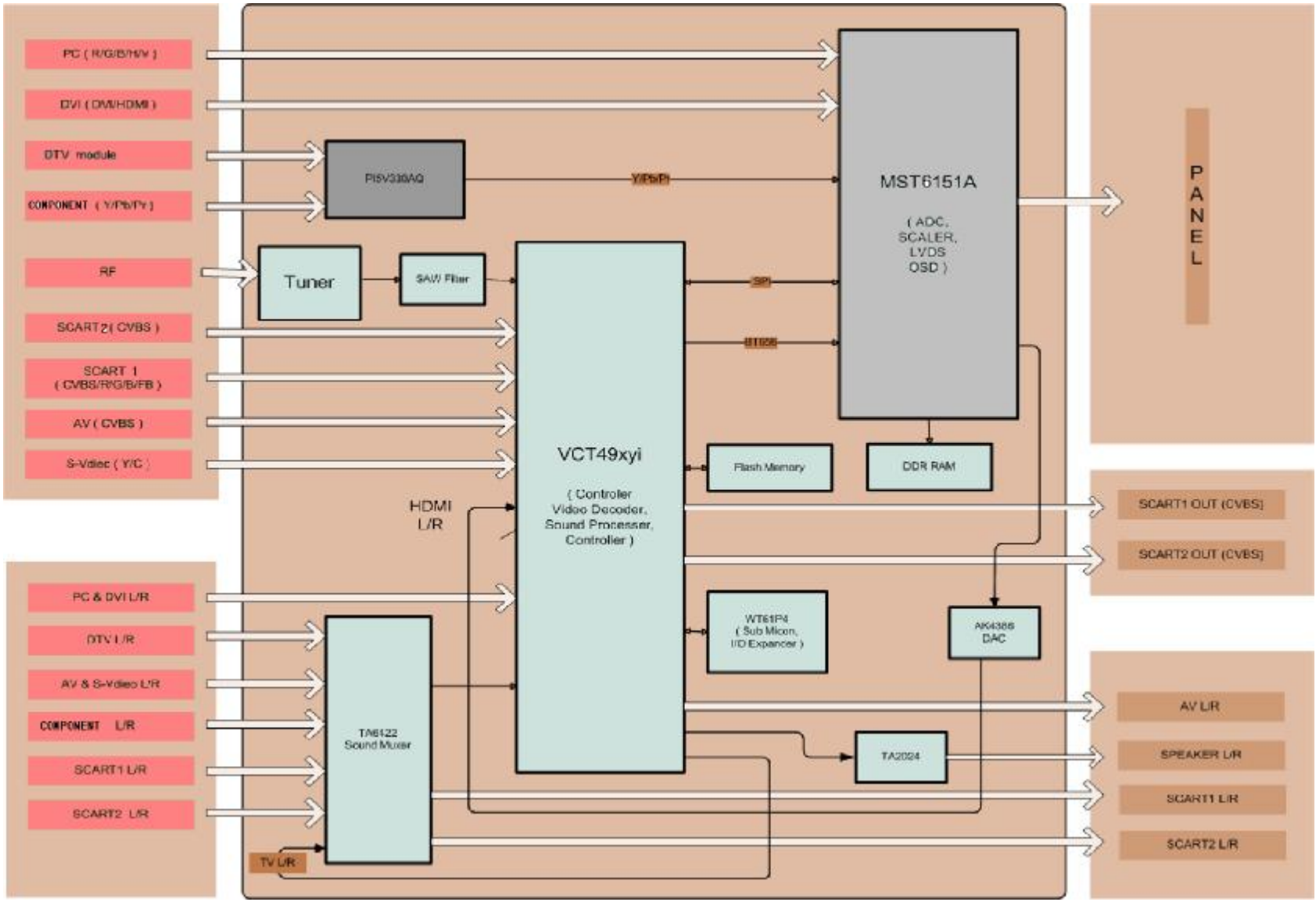
LC4201E PART LIST

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
1	1	B4204678350	KIT LAB&MAN,E420D DVB-T MZE/SKD(SILVER)	
2	1	6316349421	STICKER RoHS ELO ALL	
3	1	6316349467	STICKER,SHIPPING LABEL E420D MARANTZ	
4	1	6316379729	BACK LABEL E370D/E420D MARANTZ	
5	1	6320239072	MANUAL ASS'Y E370D/E420D MARANTZ/DVB-T	
6	1	6243037901	MANUAL PE BAG	
7	1	6320240108	MANUAL U/G, E370D/E420D MARANTZ/DVB-T	
8	1	B4210348200	SCREW ASSY,E420D HIE SKD	
9	12	5001000681	SCR-WSP,MC(+)3*5[S]	
10	4	5001000684	SCR-WSP,MC(+)3*8[S]	
11	4	5001000686	SCR-BIN,MC(+)4*10[B]	
12	4	5001000712	SCR-BIN,MC(+)8*14[B]	
13	6	5001000714	SCR-BIN,MC(+)4*10[S]	
14	4	5001000716	SCR-BIN,(T/SP)MC(+)4*6[S]	
15	4	5001000727	SCR-HEX,UNC #4-40*11.8[S]	
16	8	5001000747	SCR-BIN(SP),MC(+)4*10[S]	
17	6	5001000752	SCR-BIN(SP),MC(+) 4*16[B]	
18	5	5004000197	SCR-BIN,TT2(+)3*10[S]	
19	11	5004000223	SCR-BIN,TT2(+)3*8[B]	
20	30	5004000228	SCR-BIN,TT2(+)4*14[B]	
21	4	5401000087	WASH-PL,8[B]	
22	4	5402000002	WASH-SP,8[B]	
23	1	6128010197	GASKET EMI,12x15Tx30	
24	5	6210107121	AL TAPE, 40X70	
25	1	B4210348201	ETC ASSY,E420D HIE SKD	
26	2	B4008500100A	CABLE TIE	
27	1	6128010215	GASKET EMI,20X21TX45	
28	1	6128010232	FABRIC GASKET,10x9Tx15(FAB)	
29	1	6210107111	AL TAPE, 80X80	
30	2	6210109600	AL TAPE,35x35	
31	1	6210109700	FABRIC TAPE,30x100	
32	4	6223088700	WIRE SADDLE,H=18.2	

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
33	1	6225033900	INSULATION SHEET,E420	
34	1	E4205029703	MAIN ASSY(M1)/L,E420 DVB-T(W/O PCB'A)	
35	1	3010701072	IR B/D ASSY,E SERIES DVB-T	
36	1	3725005523	CONN-A,15P POWER CABLE/Q320 ATSC	
37	1	3725005561	CONN-A,6P ATV/DTV VIDEO CBL/Q320 DVB-T	
38	1	3725005638	CONN-A,INVERTER MASTER CBL 400MM E420	
39	1	372500563810	CONN-A,INVERTER SLAVE CBL 800MM E420	
40	1	3725005664	CONN-A,MAIN PWR SWITCH CBL 400MM E MODEL	
41	1	3725005668	CONN-A,LG LVDS CBL E370 DVB-T	
42	1	3725005676	CONN-A,OSD CBL 42",46" E-SERIES JPN/DVB	
43	1	3725005677	CONN-A,SPK CBL-L 42/46" E-Series JPN/DVB	
44	1	372500567701	CONN-A,SPK CBL-R 42/46" E-Series JPN/DVB	
45	1	E42077080050	CBL-PWR,BK WALL EUROPE 1.83MT	
46	1	3010701037	REMOTE CONTROL ASSY,DVB-T KRC-61	
47	1	3010701056	KEY B/D ASSY,E-SERIES JPN/DVB-T	
48	1	3550100152	SPEAKER,E420D BOTTOM	
49	1	361020014201	PWR B/D ASSY,42",46" E-Series	
50	1	372500531201	CONN-A,PAL CABLE 3.0M MALE <-> FEMALE	
51	1	6101235880	MAIN FRAME ASSY,E420D DVB-T SKD(8)	
52	1	6101235800	MAIN FRAME ASSY,E420 DVB-T	
53	1	6101234900	MAIN FRAME,E420/E460	
54	4	6128014100	GASKET EMI,20X16TX70(FAB,PLP)	
55	0.13	6301208900	SKD BOX E420 M,F ASSY 580X265X330(예일)	
56	2	6110291580	BRKT BEAM E420 SKD(20)	
57	1	6110291500	BRKT BEAM,E420	
58	0.05	6301208901	SKD BOX E420 BRKT BEAM 670X460X145(예일)	
59	1	6110291880	PORT BRKT BOTTOM,E420 SKD(60)	
60	1	6110291800	PORT BRKT BOTTOM E420	
61	0.02	6301208902	SKD BOX E420 BRKT BTM 600X150X110(화인)	
62	1	6110291980	SIDE BRKT,E370 SKD(200)	
63	1	6110291900	SIDE BRKT,E420	
64	0.005	6301208000	SKD BOX,E370 SIDE BRKT 350x350x150(휴먼)	
65	1	6110292180	STAND BEAM,E420 SKD(14)	
66	1	6110292100	STAND BEAM,E420	

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
67	0.07	6301208903	SKD BOX E420 S_BEAM 645X240X165(예일)	
68	1	6201351781	COVER REAR,E420(NO LOGO) SKD(7)	
69	1	6201351702	COVER REAR,E420(NO LOGO)	
70	0.13	6301208904	SKD BOX E420 COVER 1180X540X680(세화)	
71	1	6201352080	CAP PORT SIDE,E420 SKD(400)	
72	1	6201352000	CAP PORT SIDE,E420	
73	0.003	6301207500	SKD BOX,E370 CAP PORT SIDE 500x500x350(	
74	1	6201353681	STAND BASE ASSY,E370 SKD(8)	
75	9	5004000217	SCR-BIN,TT2(+)4*10[S]	
76	1	6101235000	STAND BASE FRAME SQUARE,E420	
77	1	6201352100	STAND BASE SQUARE,E420	
78	4	6261050600	RUBBER FOOT Φ19.0 4.0T	
79	5	6261050700	RUBBER FOOT Φ19.0 4.5T	
80	0.125	6301208200	SKD BOX,E370 BASE ASSY 570x215x320(동산)	
81	1	6201353684	STAND BODY ASSY(BK2,SP) E370D SKD(6)	
82	7	5004000248	SCR-BIN,TT2(+)4*14[S]	
83	7	5004000252	SCR-FLT,TT2(+)4*14[S]	
84	1	6110292600	BODY SQUARE,E420	
85	1	6110292702	BODY BRKT(BK,SP) E420	
86	1	6115029301	SWIVEL ASSY,E420	
87	1	6110292800	SWIVEL TOP BRKT,E420	
88	1	6110292900	SWIVEL BOTTOM BRKT,E420	
89	1	6120342700	SWIVEL DECO,E420	
90	1	6201352201	BODY CAP,E420(BK)	
91	0.17	6301208100	SKD BOX,E370 BODY ASSY 520x340x240(동산)	
92	1	6201358381	COVER F,ASSY E420 DVB-T MZE SKD(12)	
93	1	6201358302	COVER FRONT ASSY,E420 DVB-T MZE	
94	1	6201351600	COVER FRONT,E420	
95	1	6201361600	DECO PANEL E420(ACRYL)/MZE	
96	1	6210336400	LOGO PLATE (PDP)	
97	0.08	6301208904	SKD BOX E420 COVER 1180X540X680(세화)	
98	4	6223088400	42INCH PDP BOX HOLDER	
99	1	6242034500	BOTTOM PORT LABEL,E420 DVB-T	
100	1	6242034600	SIDE PORT LABEL E420 DVB-T	

NO	QUANTITY	PART NUMBER	DESCRIPTION	REMARK
101	1	6243039800	PE BAG(SET),1280X1300 HDPE DOUBLE	
102	1	6253130200	CUSHION TOP "L",E370	
103	1	6253130201	CUSHION TOP "R",E370	
104	1	6253130300	CUSHION BOTTOM "L",E370	
105	1	6253130301	CUSHION BOTTOM "R",E370	
106	1	6301204100	ACCESSORY BOX,Q400	
107	1	6301208500	CTN BOX,DW-2 E420D BOTTOM	
108	1	6301208701	CTN BOX,DW-2 E420D MARANTZ	
109	1.5	6316349238	LABEL SHIPPING,ELO(W/T)-80*40	



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Size C	Document Number E42095503	Rev 1
Date: Monday, June 05, 2006	Sheet 2 of 13	

Schematic Diagra

CHASSIS NO : LT-3211

Date:2006.05.18

Title: EXXX SCHEMATIC DIAGRAM COVER PAGE		
Size: B	Document Number: E42095502	Rev: 01
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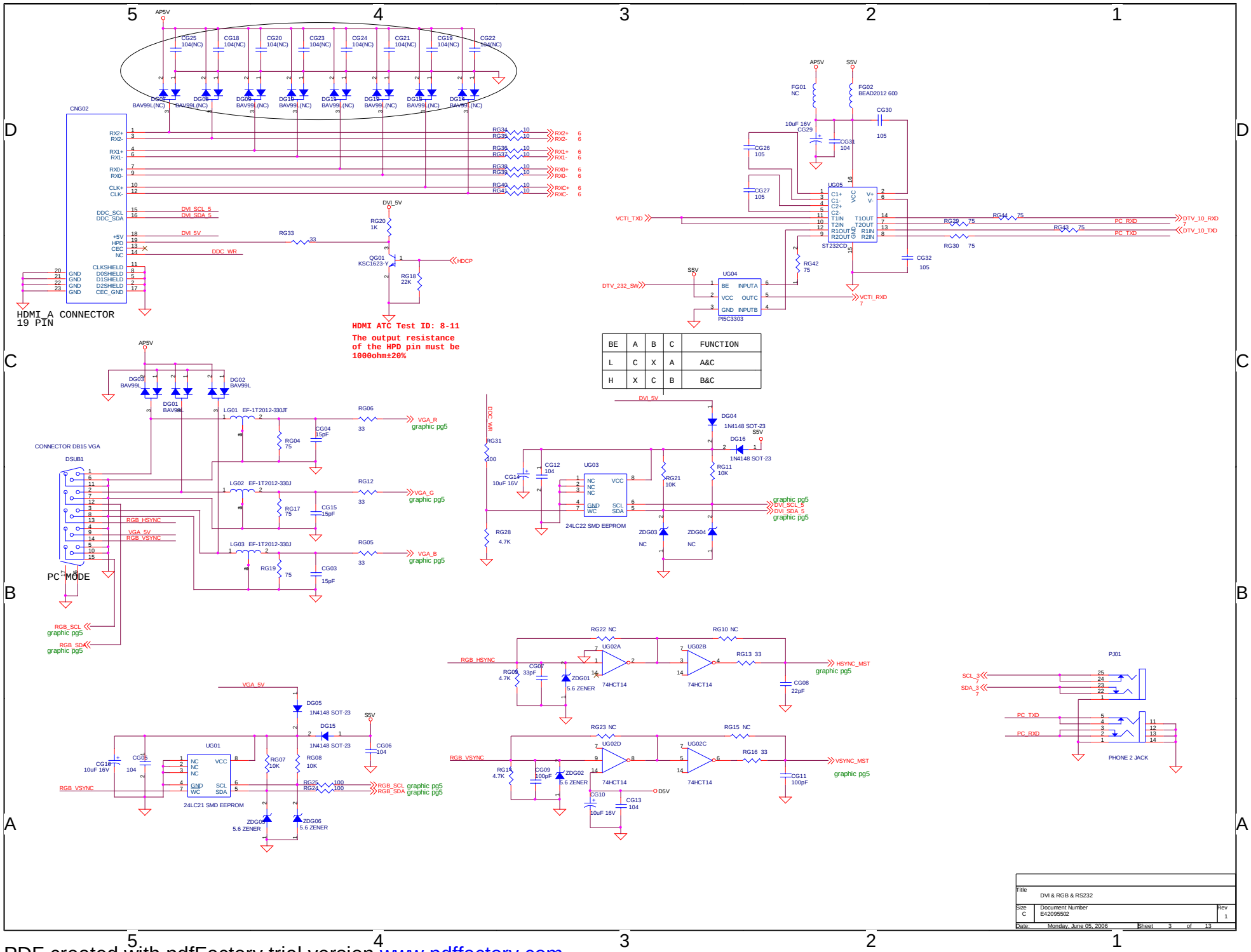
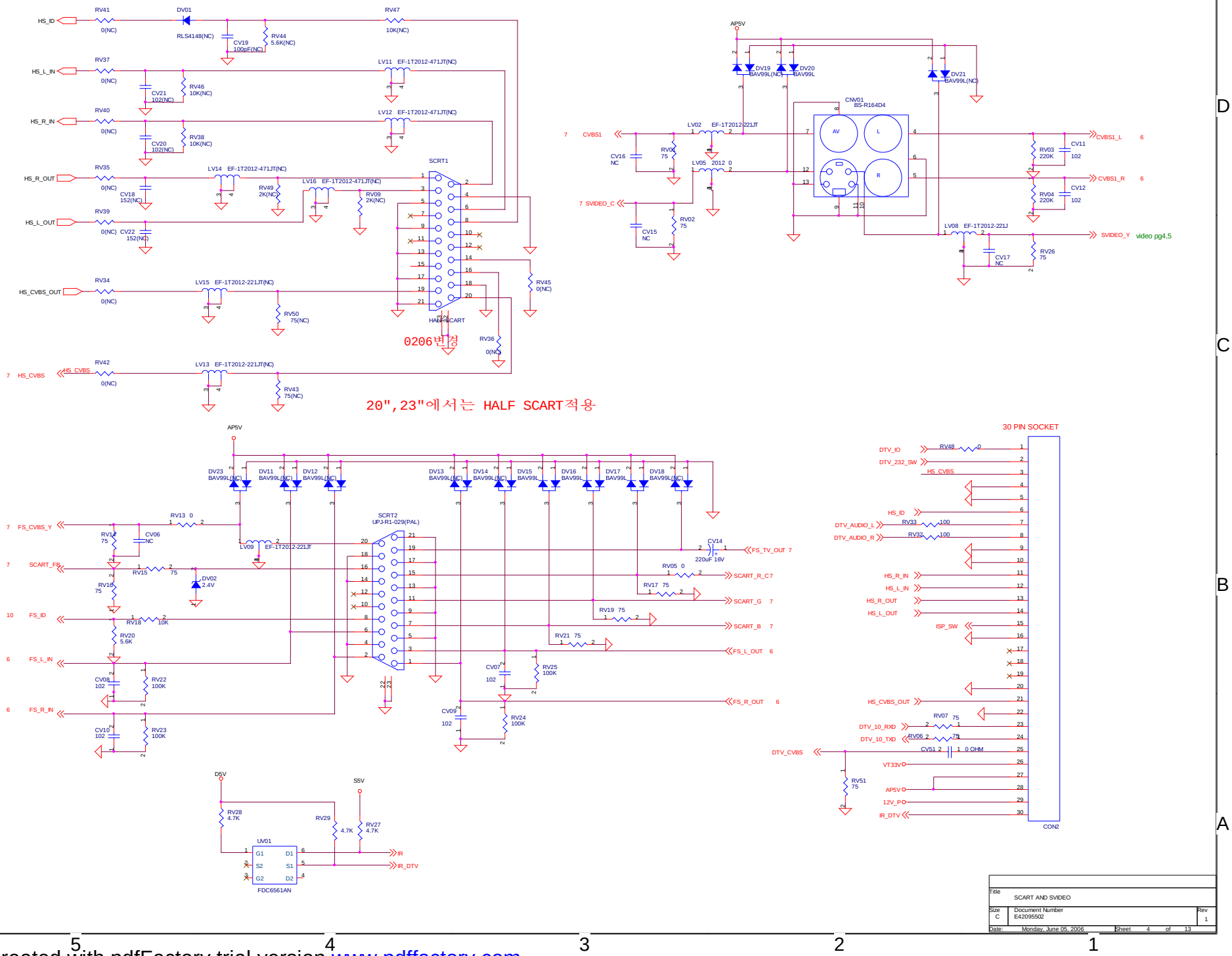
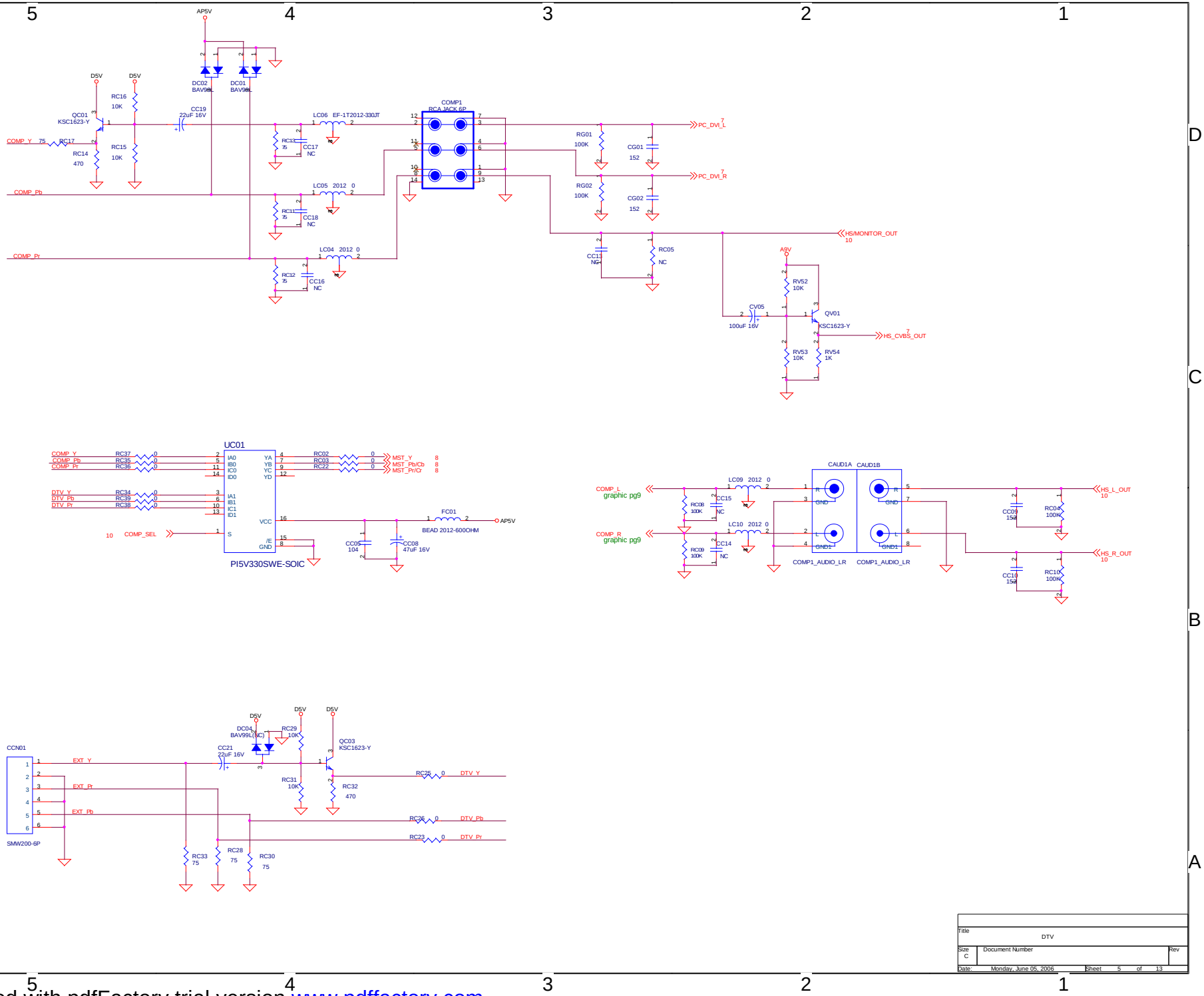


BE	A	B	C	FUNCTION
L	C	X	A	A&C
H	X	C	B	B&C





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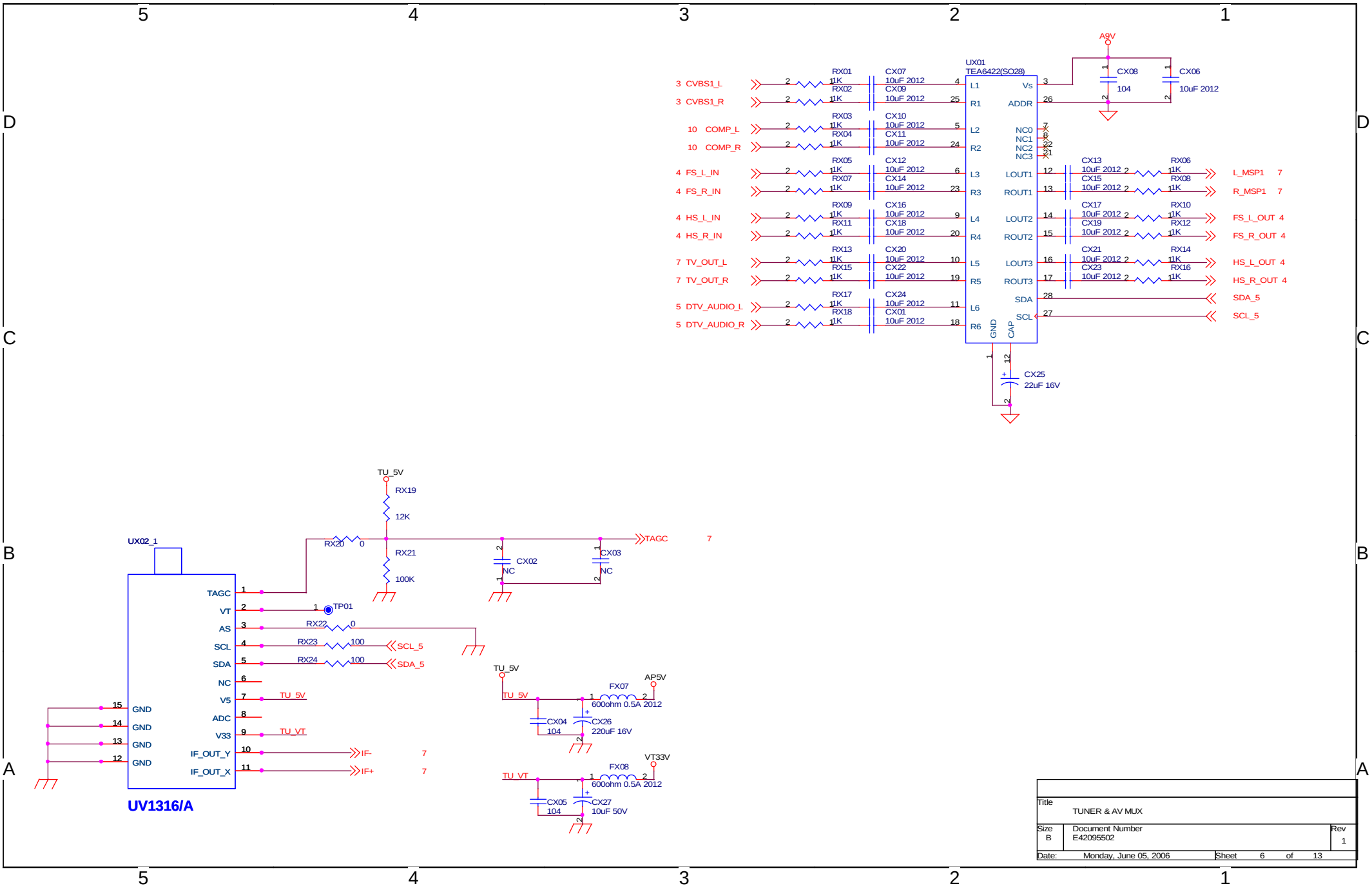

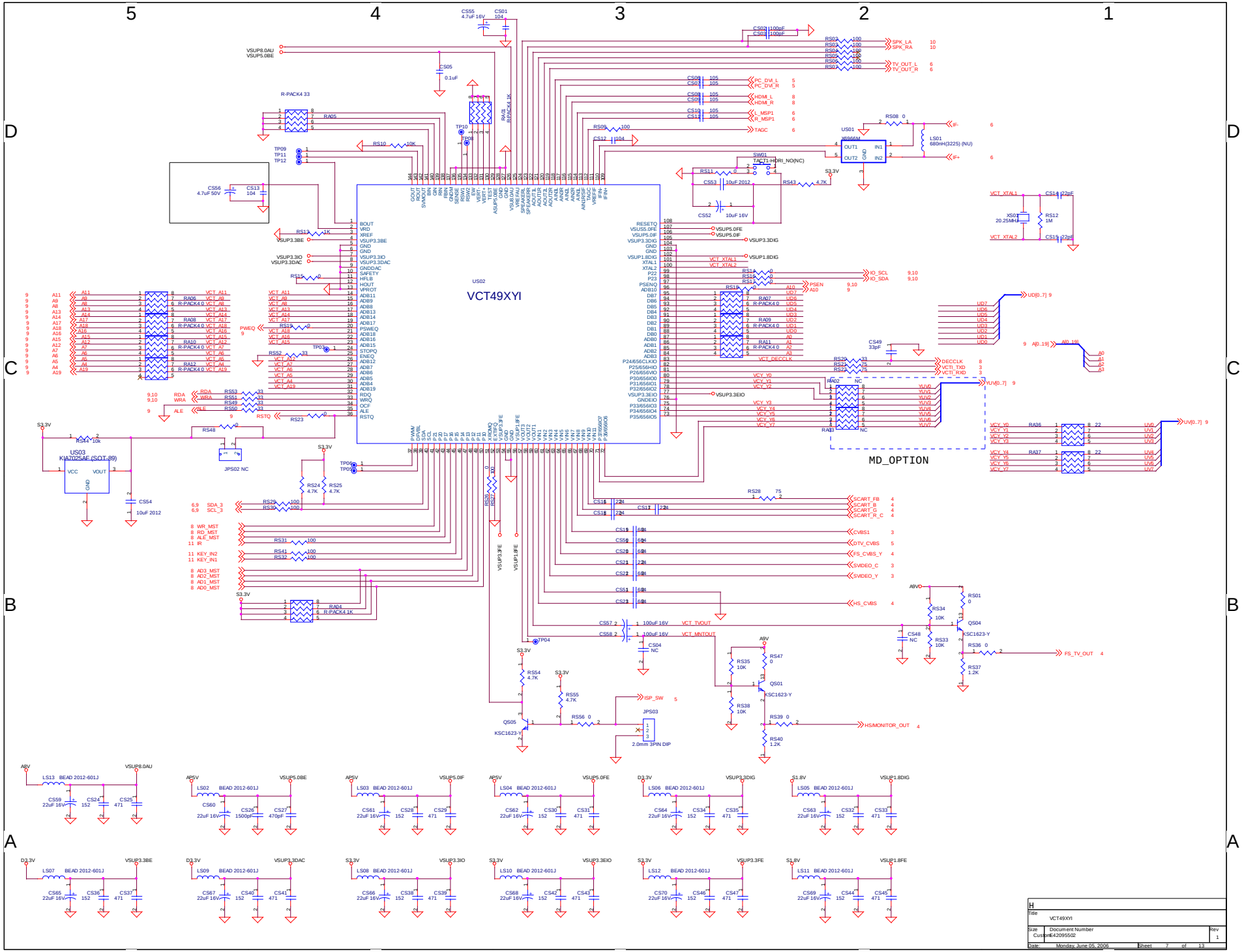

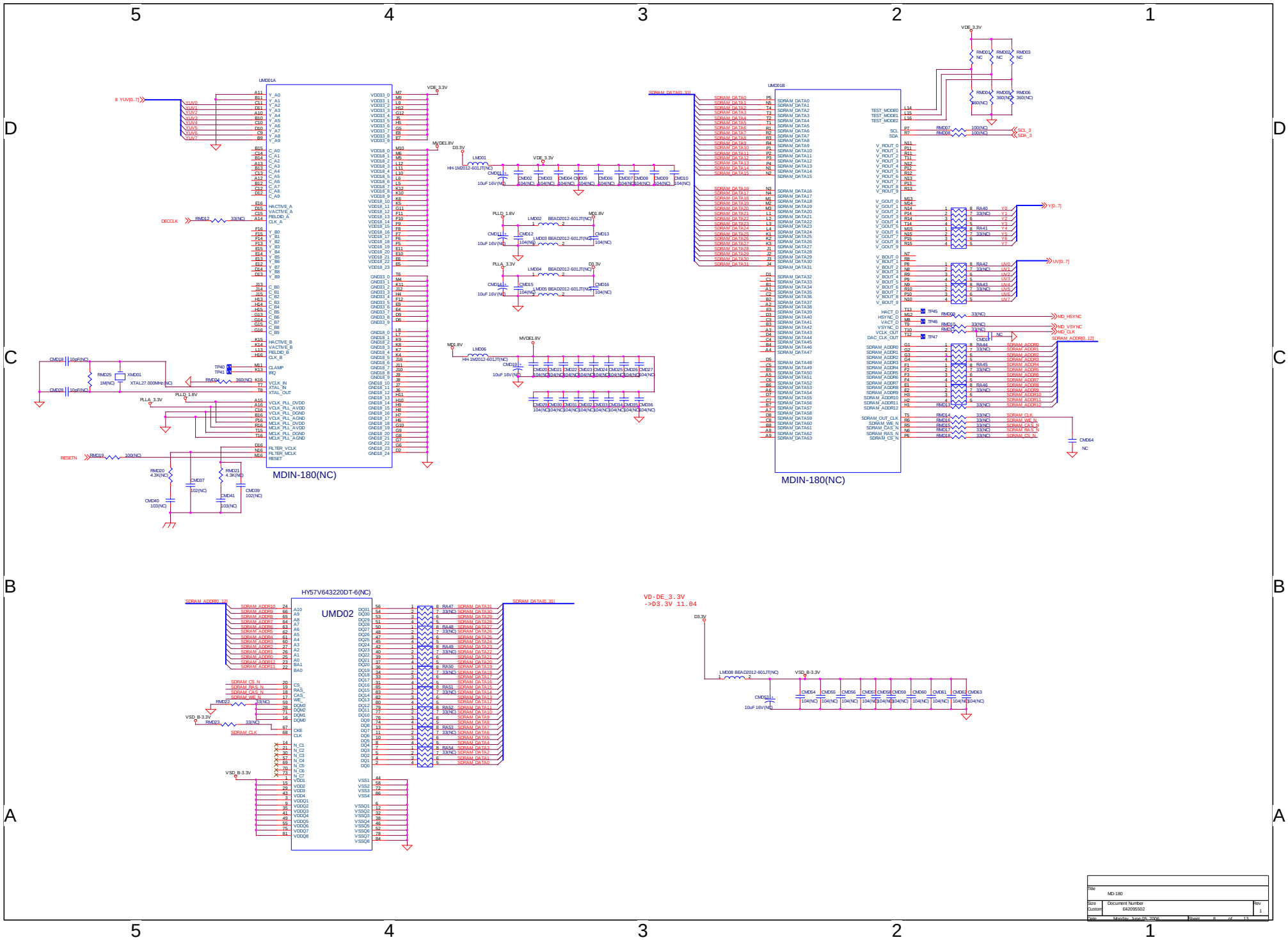

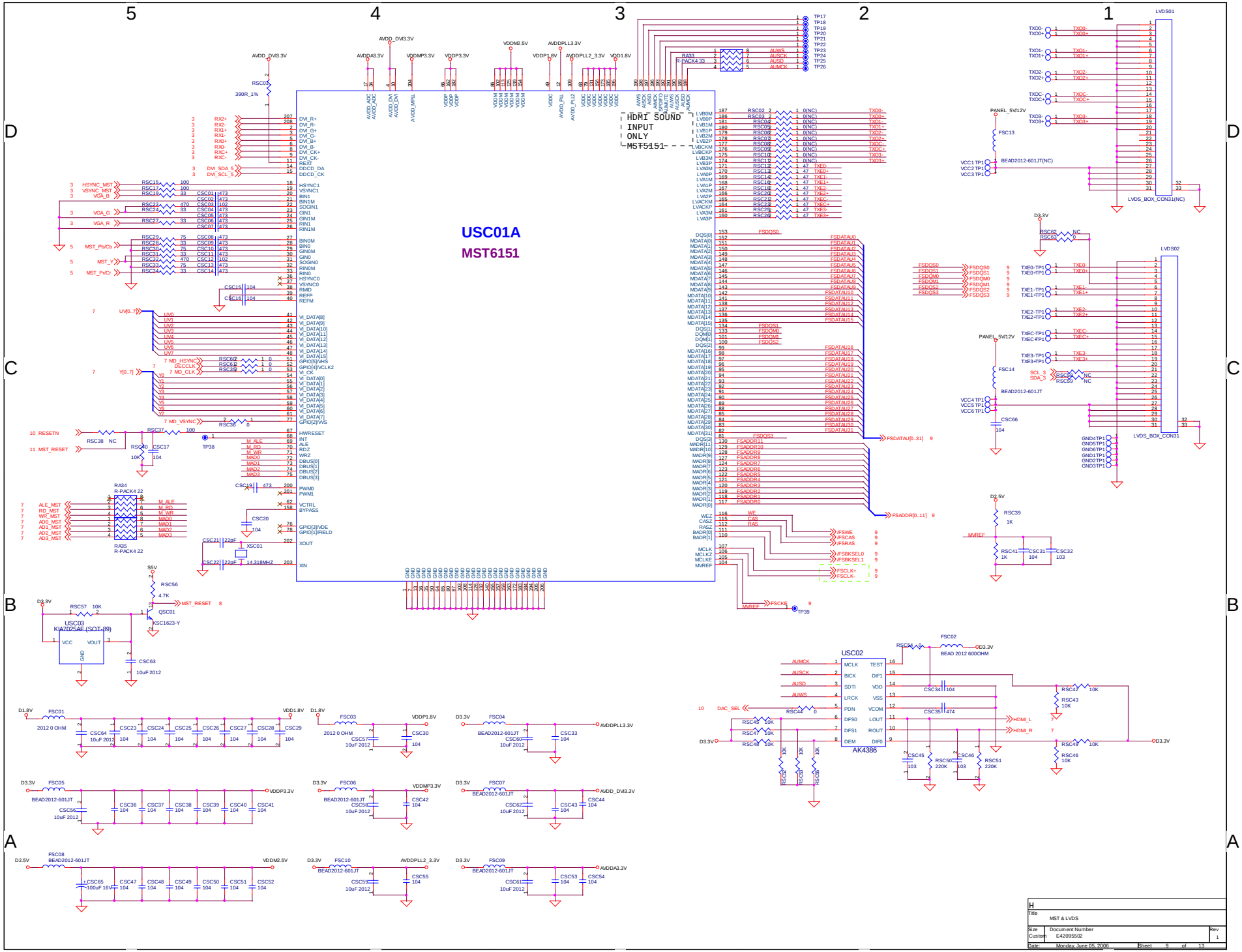

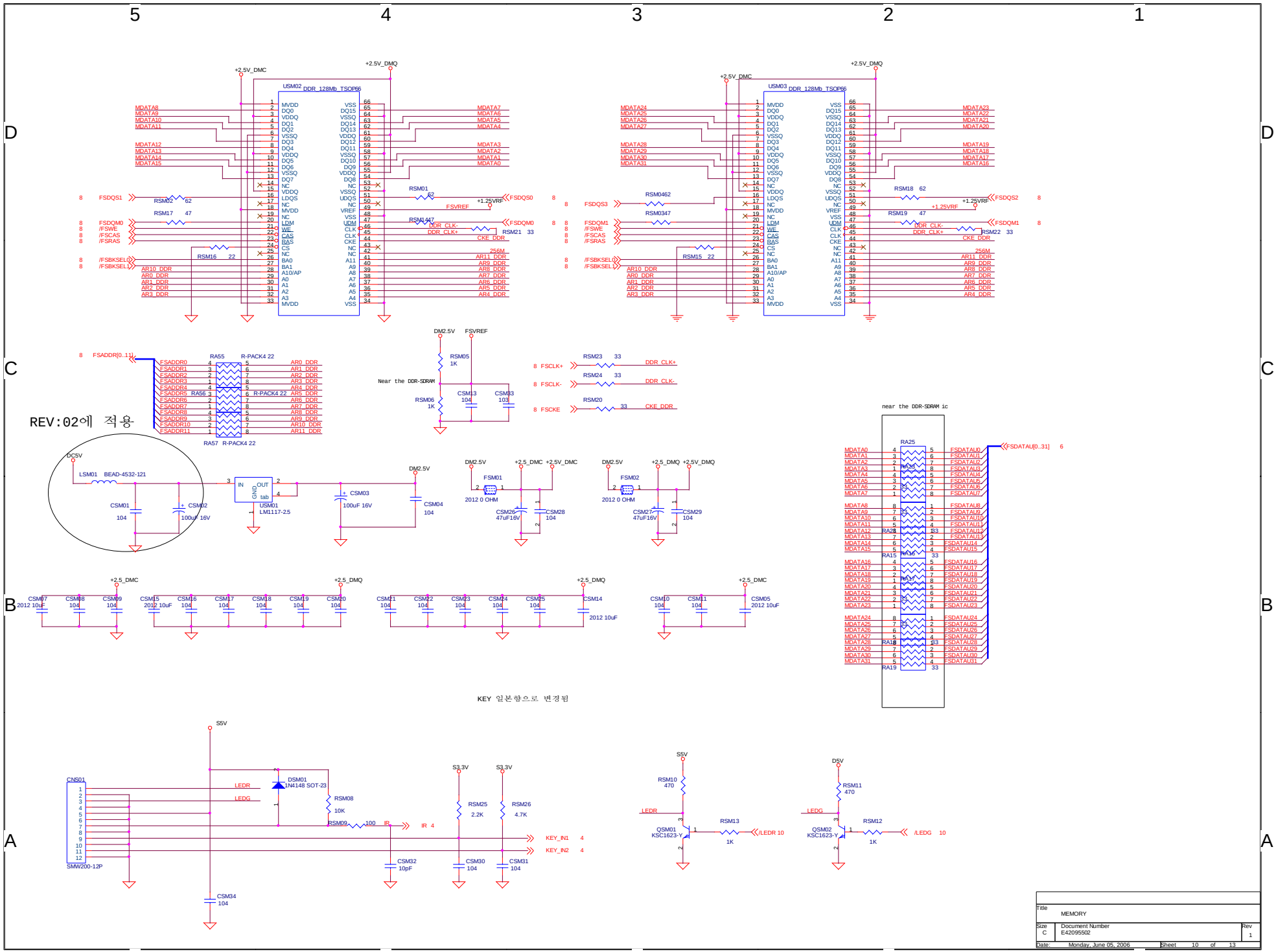

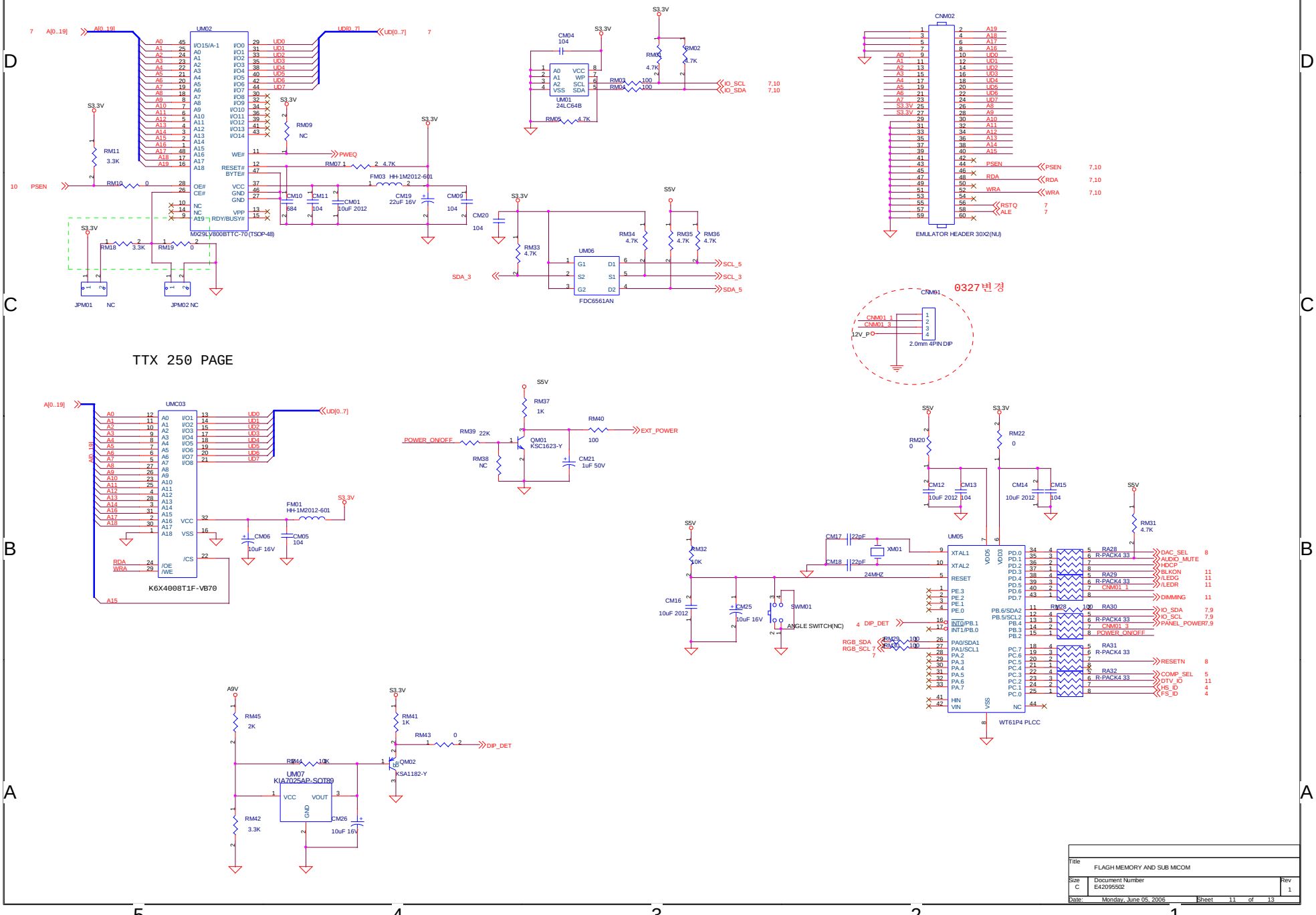

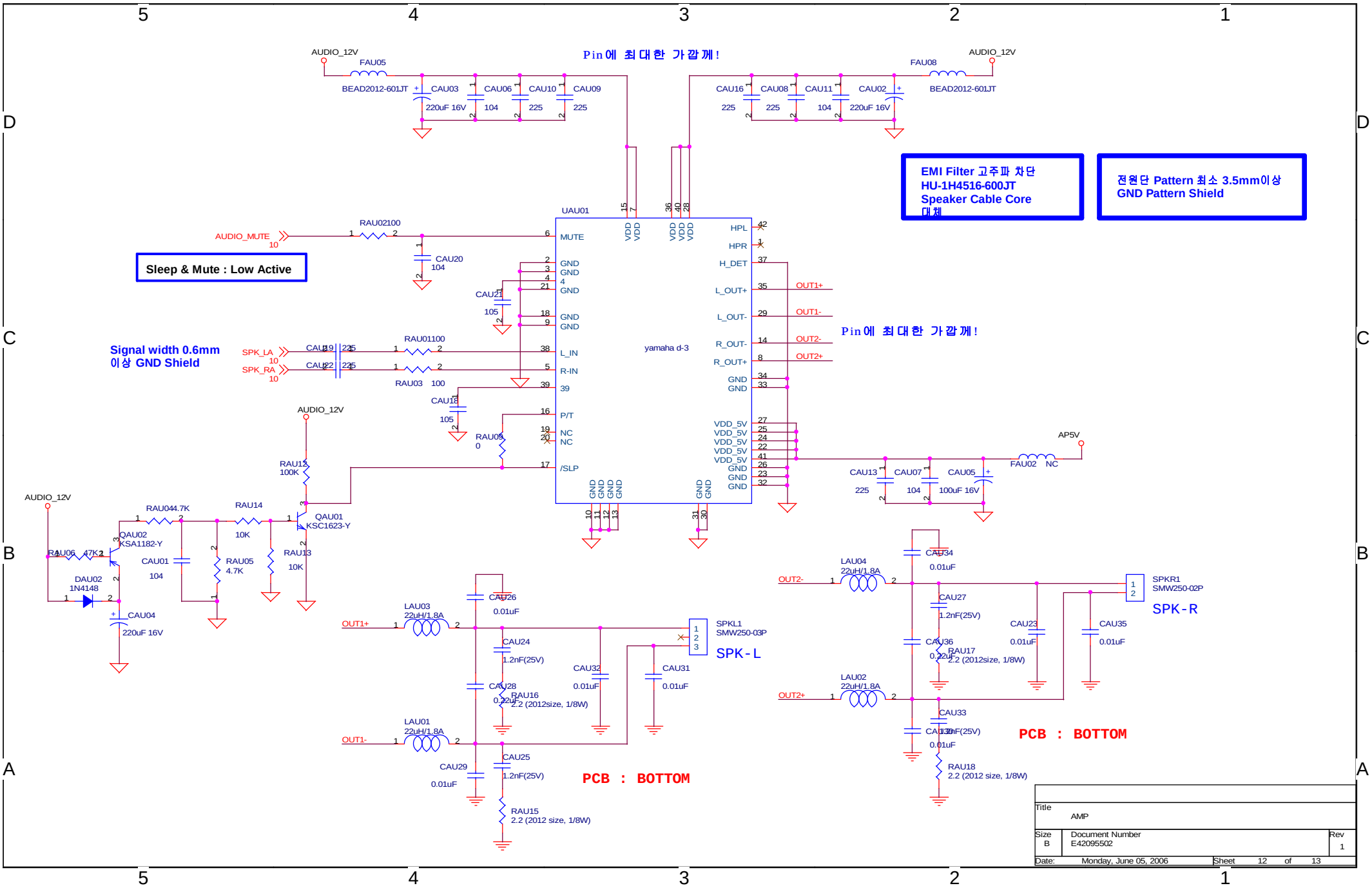

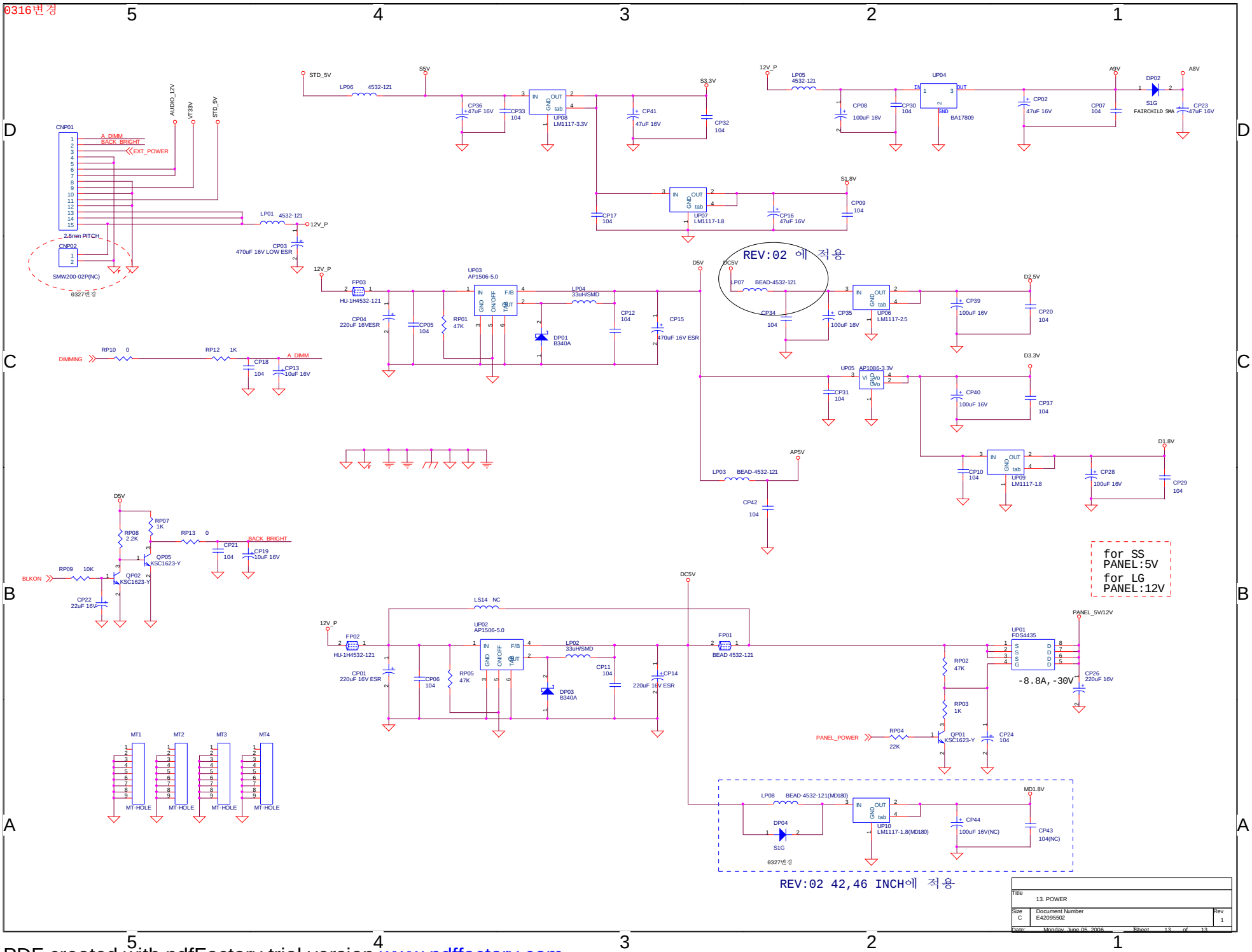

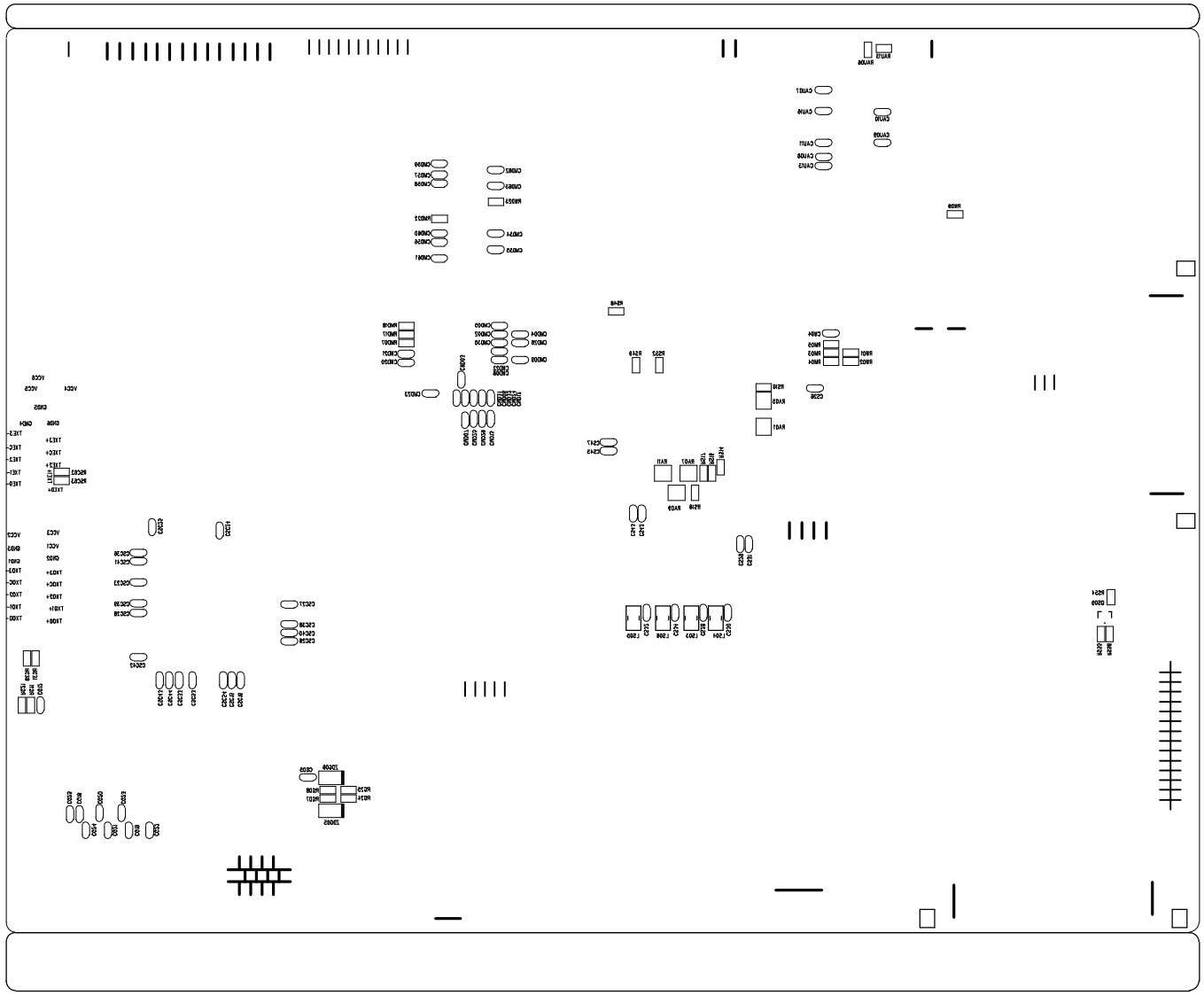

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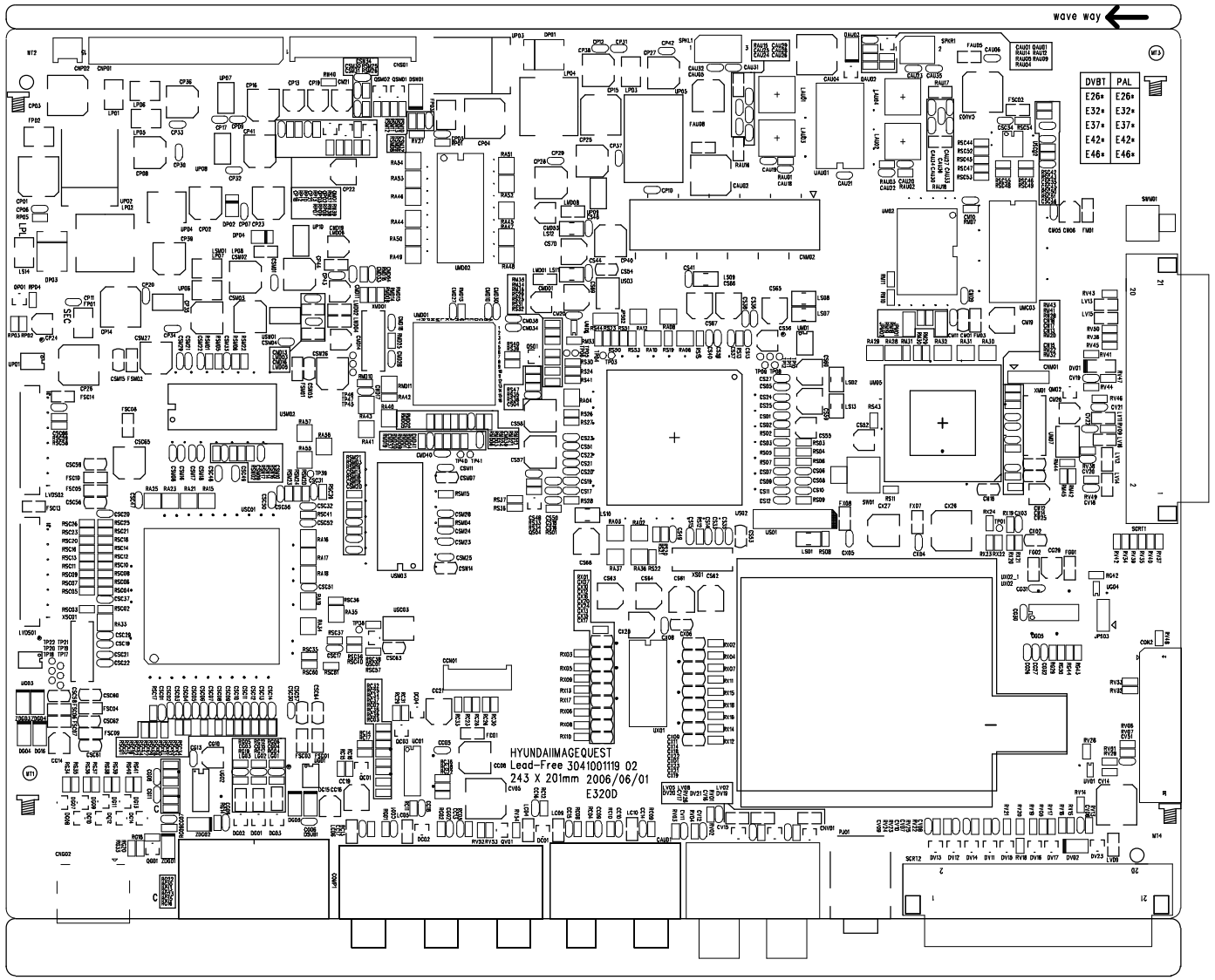

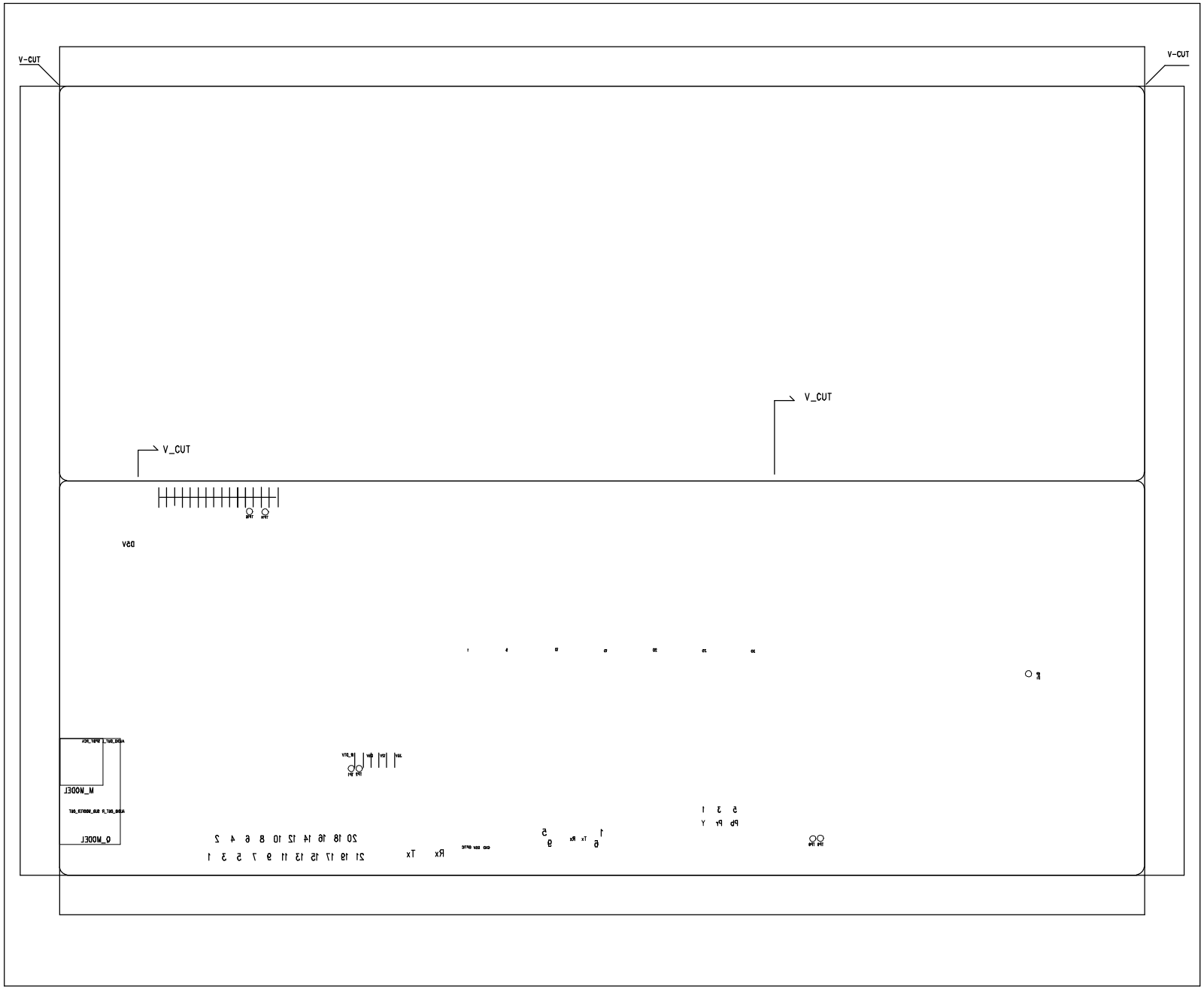

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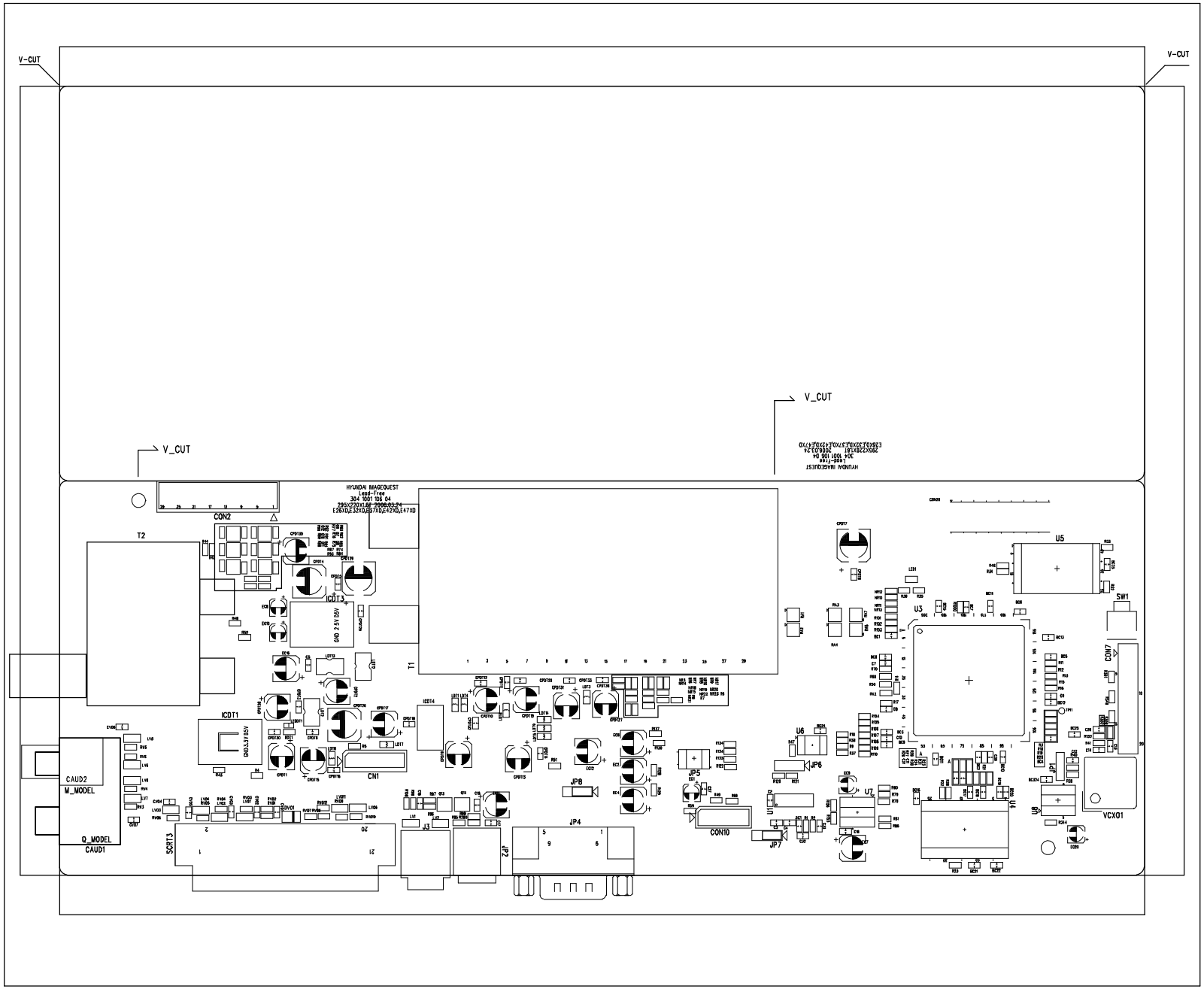

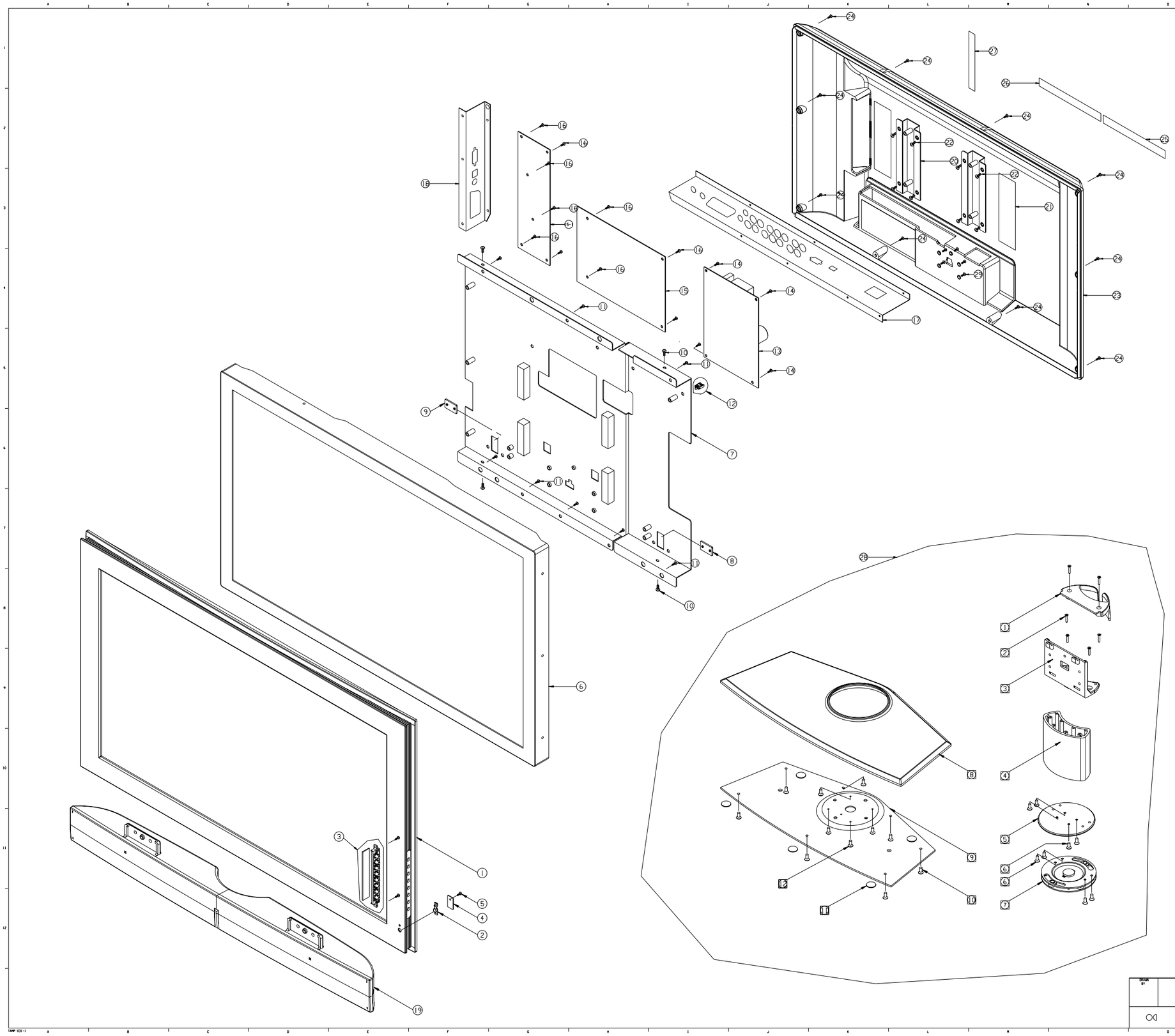

29	5001000752	SCREW	MC(•)4•16[S]	5	
28	62013525	STAND ASSY	———	1	
1	6201352700	CABLE CAP E320	ABS(94V-0)	1	
2	5004000248	SCREW	SCR-BIN TT(2) 4X14[S]	6	
3	6110293002	BODY BRKT E320	ALDC 12S(BK.SP)	1	
4	6110293100	BODY FRAME E320	ALDC 12S(SANDING)	1	
5	6110293200	SWIVEL DECO E320	AL5052 3T(DIA CUT)	1	
6	5004000242	SCREW	SCR-FLT.TT2(•) 4X11[S]	8	
7	6115029100	SWIVEL ASSY	———	1	
8	6201352600	STAND BASE SQUARE	ABS(94-HB)	1	
9	6101235100	BASE FRAME SQUARE	GI 3.0T	1	
10	5004000211	SCREW	SCR-FLT.TT2(•)4•8[S]	7	
11	6261050800	RUBBER FOOT	RUBBER STAND	5	
12	5001000714	SCREW	SCR-BIN.MC(•)4X10[S]	4	
27	62420344	LABEL SIDE		1	
26	62420344	LABEL R		1	
25	62420344	LABEL L		1	
24	5004000228	SCREW	TT2(•)4•14[B]	10	
23	62013512	COVER REAE	ABS(94V-0)	1	
22	5004000211	SCREW	FLT.TT2(•)4•8[S]	8	
21	62103376	INSULATION	———	2	
20	61102924	WALL BRKT	EGI 0.8T	2	
19		SPK ASSY	ABS(94-HB)	1	
18	61102923	SIDE BRKT	EGI 0.8T	1	
17	61102922	PORT BRKT	EGI 0.8T	1	
16	5001000681	SCREW	MC(•)3•5[S]	10	
15-1		DTV BOARD	———	1	
15		MAIN BOARD	———	1	
14	5001000684	SCREW	MC(•)3•8[S]	4	
13		POWER BOARD	———	1	
12	62230887	WIRE SADDLE	H-18.2	3	
11	5004000228	SCREW	TT2(•)4•14[B]	8	
10	5001000730	SCREW	MC(•)4•8[S]	4	
9		SPK JACK WHITE	———	1	
8		SPK JACK RED	———	1	
7	61012346	FRAME ASSY	EGI 1.0T	1	
6	3330500315	32" MODULE	———	1	
5	5004000223	SCREW	TT2(•)3•8[B]	3	
4	30107010	IR B/D ASSY	———	1	
3	30107010	KEY PAD ASSY	———	1	
2	62200880	LENS LED	IF-850	1	
1	62013511	COVER FRONT	ABS(94V-0)	1	
	PART CODE	PART NAME	DESCRIPTION	6	REMARKS

DRAWN BY	CHECKED BY	APPROVED BY	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN mm (INCHES) TOLERANCES ARE LINEAR ANGLES RADII UNLESS NOTED ± ±	ANGLE ± / SCALE 1/N	TITLE: EXPLODED VIEW
				SIZE A2	DWG NO.